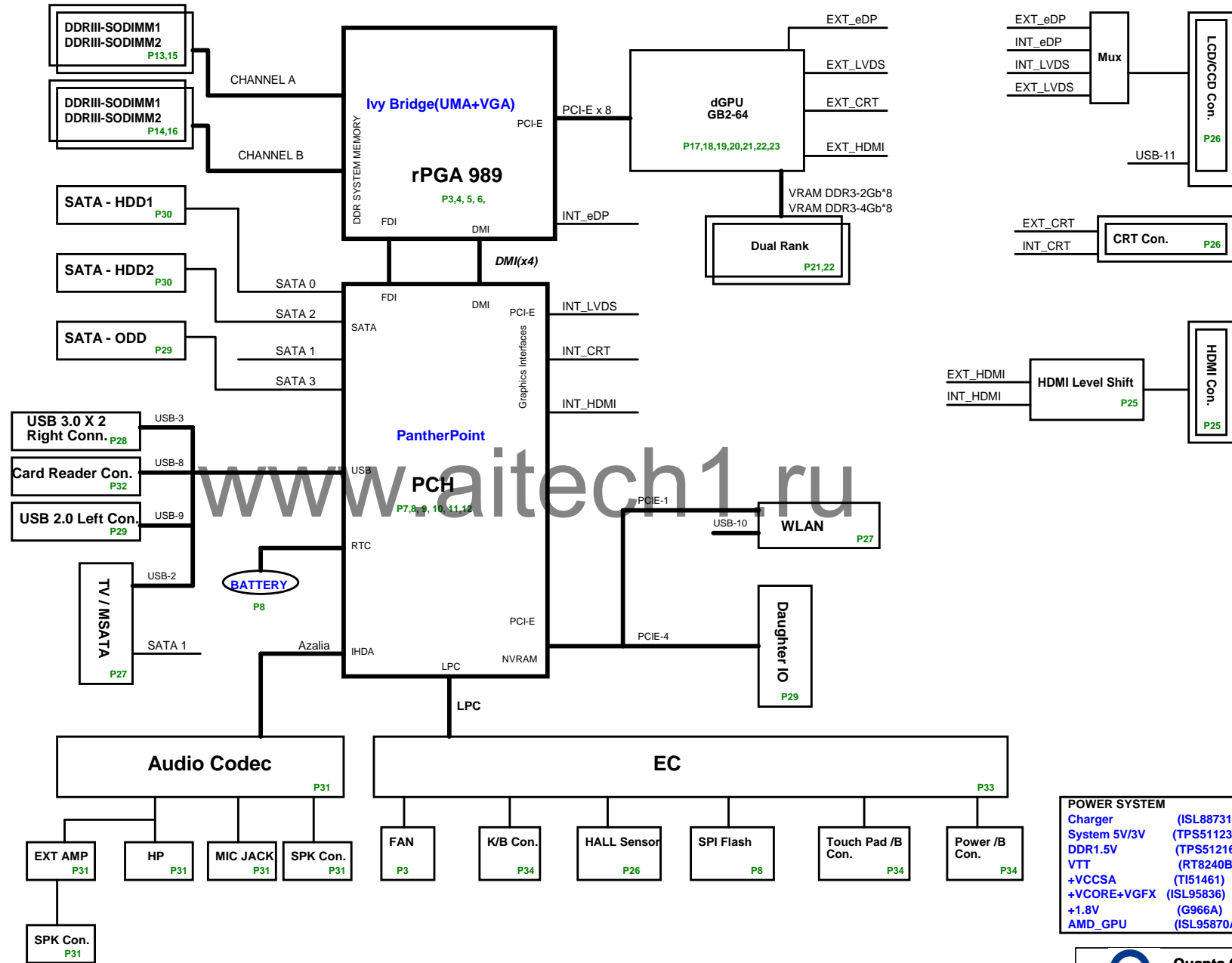
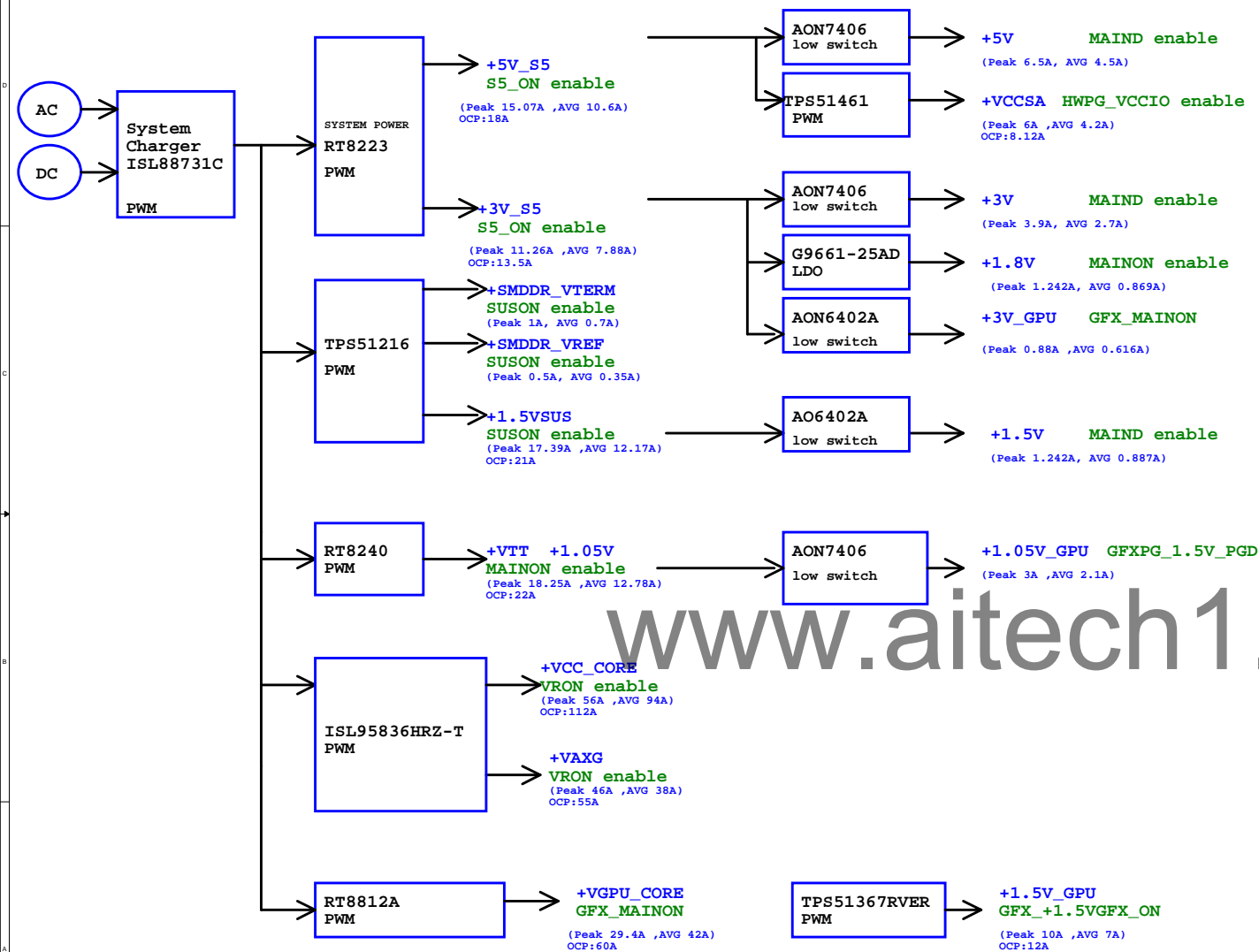


Chief River Block Diagram

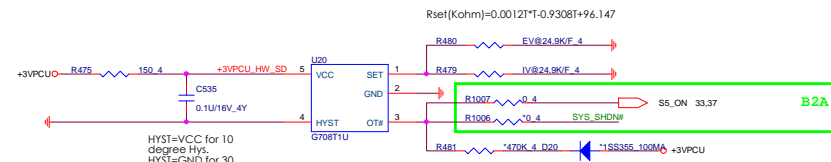
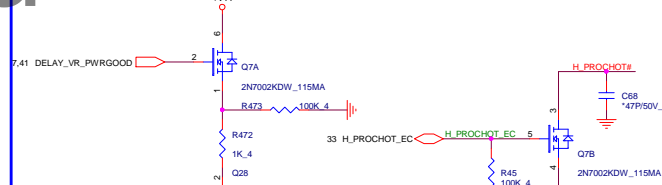
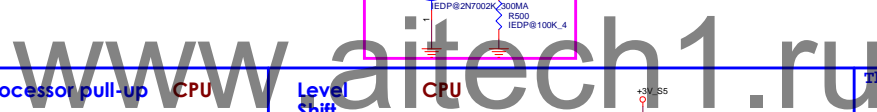
01

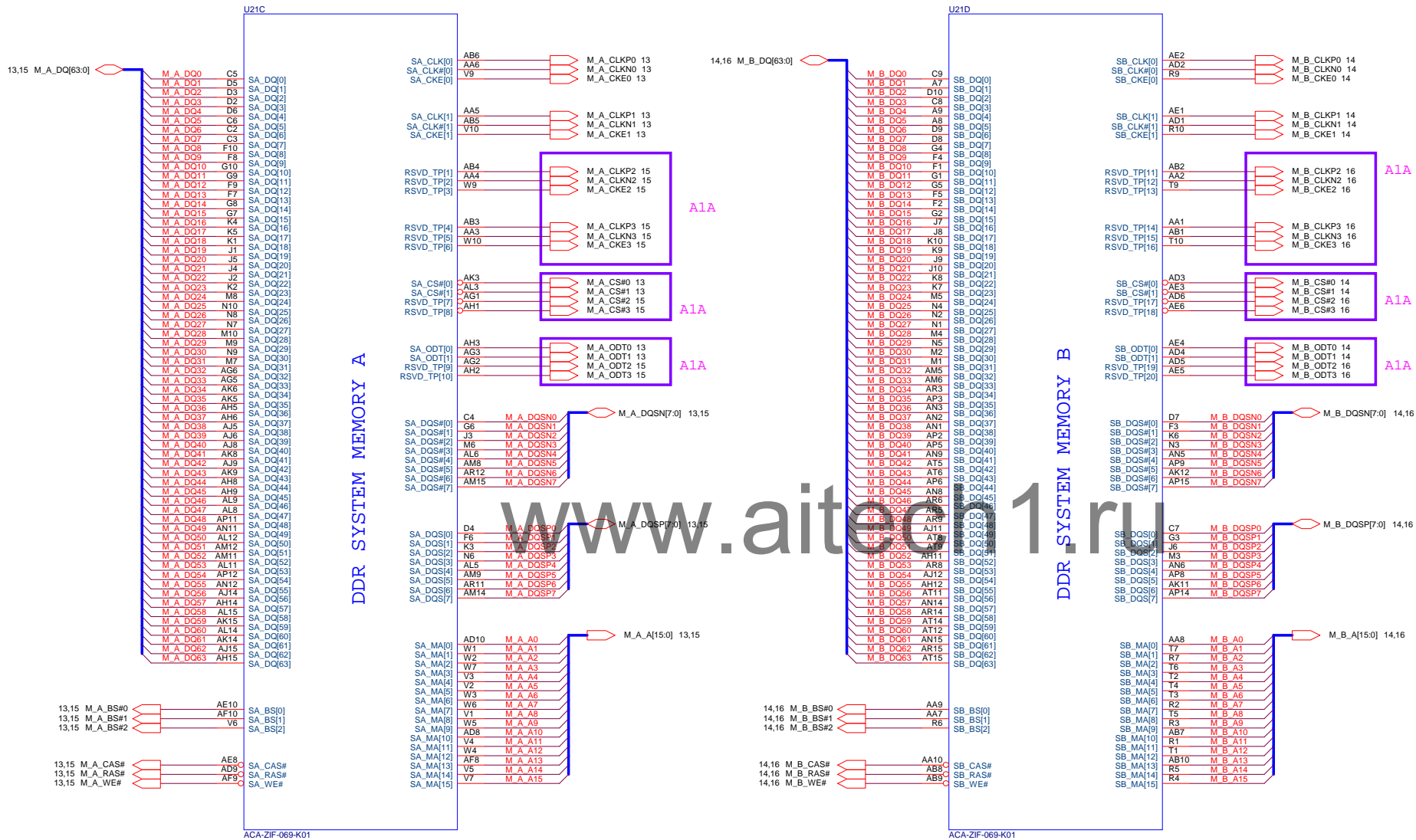


POWER SYSTEM		
Charger	(ISL88731C)	P40
System 5V/3V	(TPS51123A)	P41
DDR1.5V	(TPS51216)	P42
VTT	(RT8240BGQW)	P43
+VCCSA	(TI51461)	P44
+VCORE+VGFX	(ISL95836)	P45
+1.8V	(G966A)	P46
AMD_GPU	(ISL95870A)	P47



POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

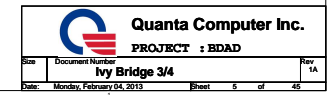


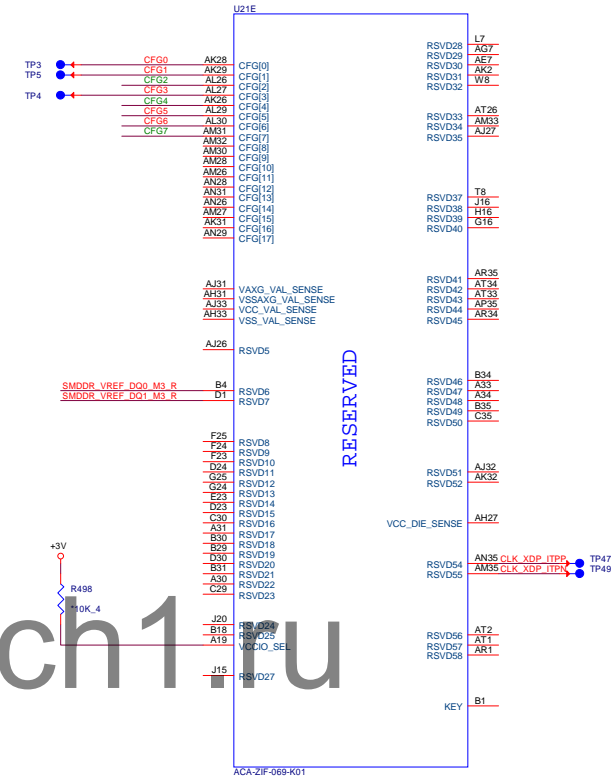


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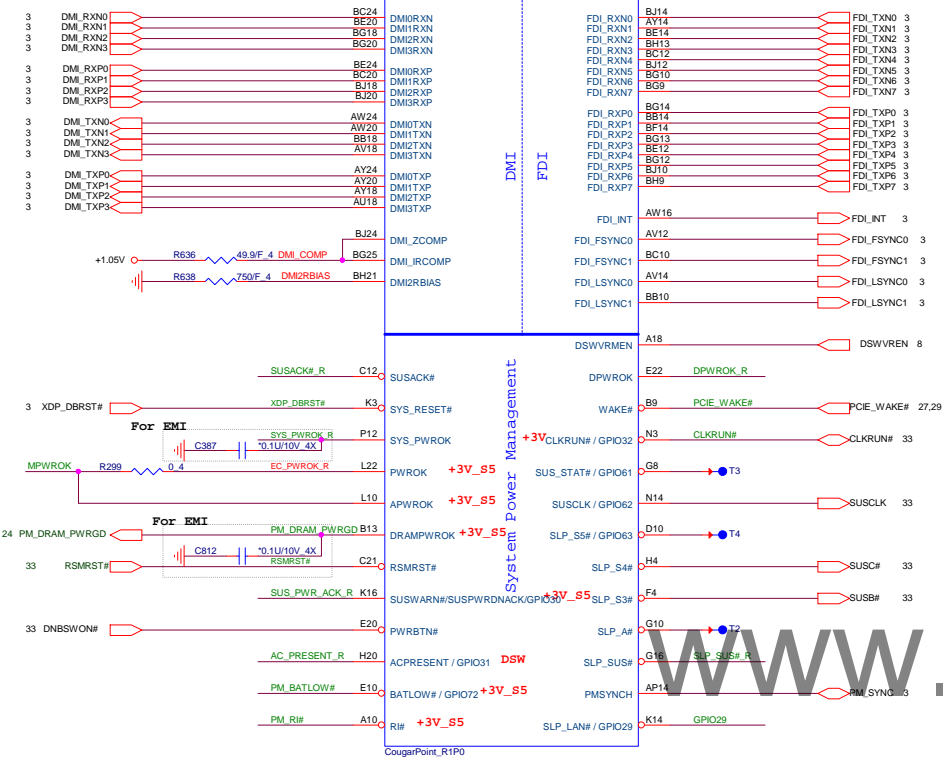
POWER





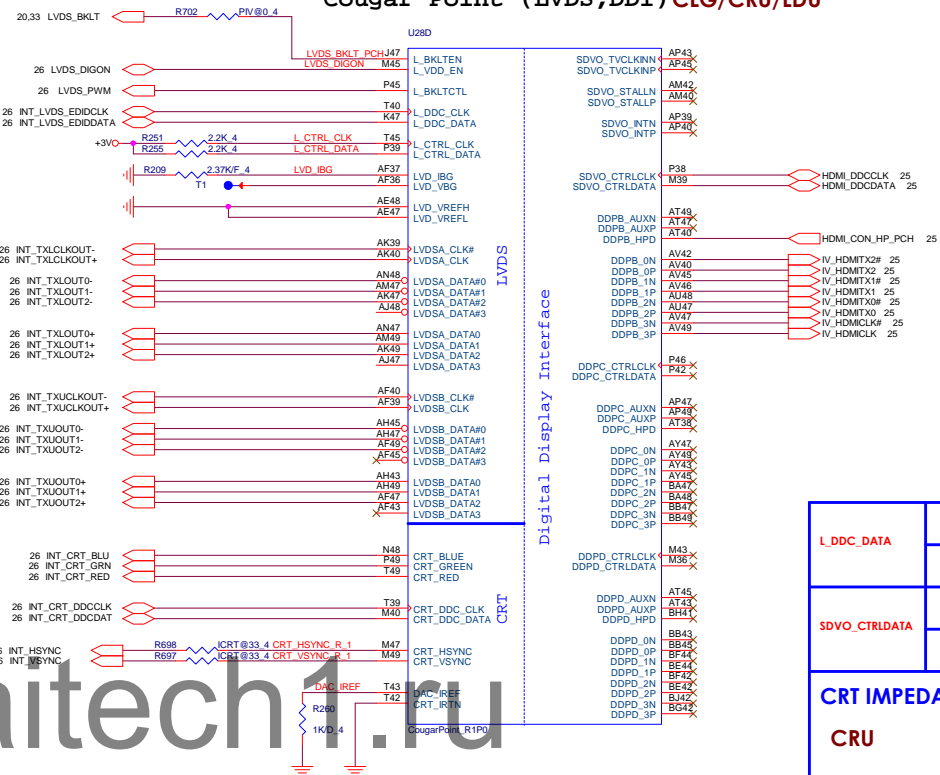
Cougar Point (DMI, FDI, PM) CLG

U28C



Cougar Point (LVDS, DDI) CLG/CRU/LDU

U28D



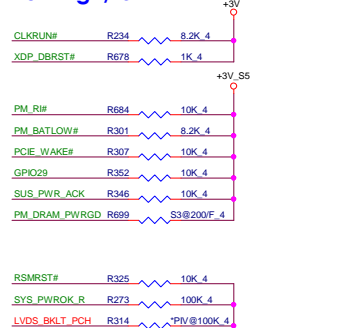
L_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

CRT IMPEDANCE MATCHING

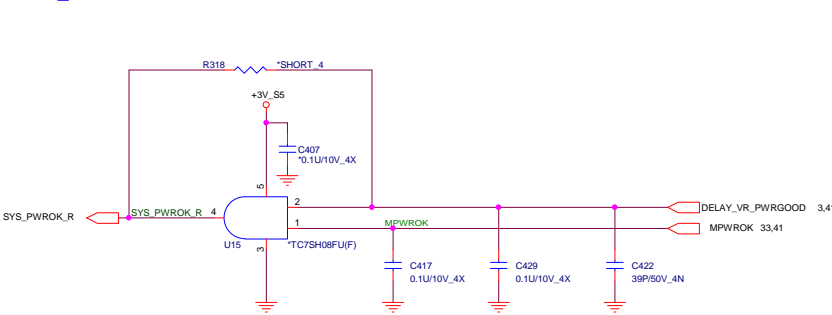
CRU



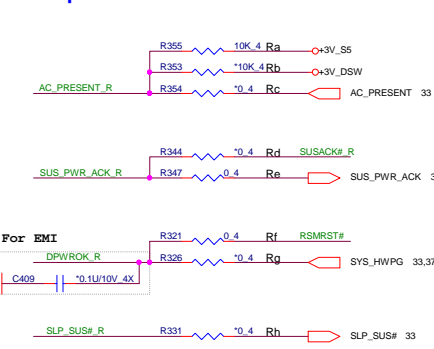
PCH Pull-high/low



System PWR_OK

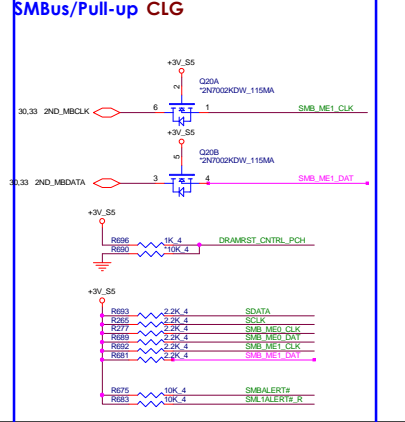
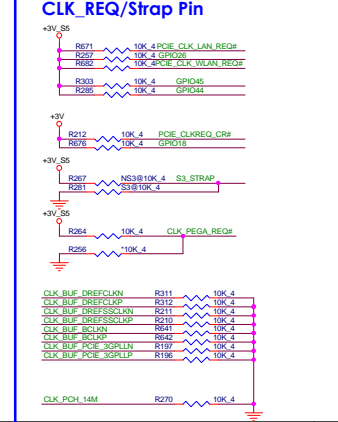
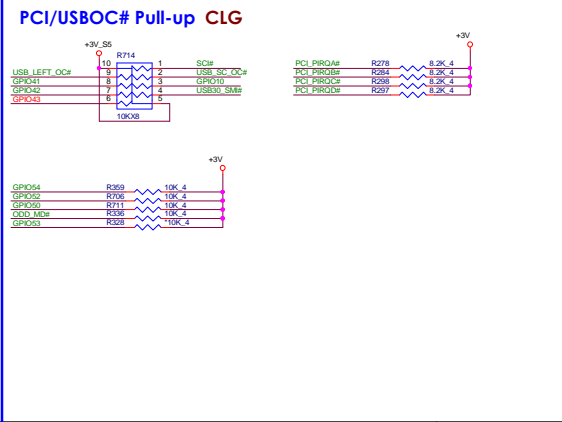
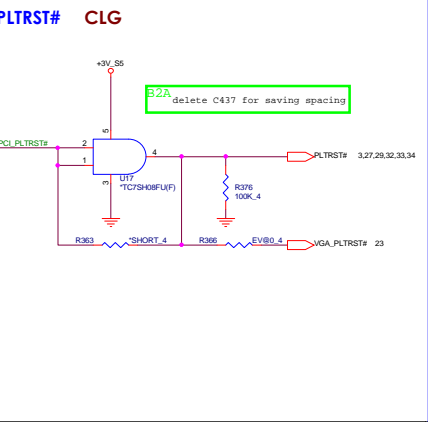
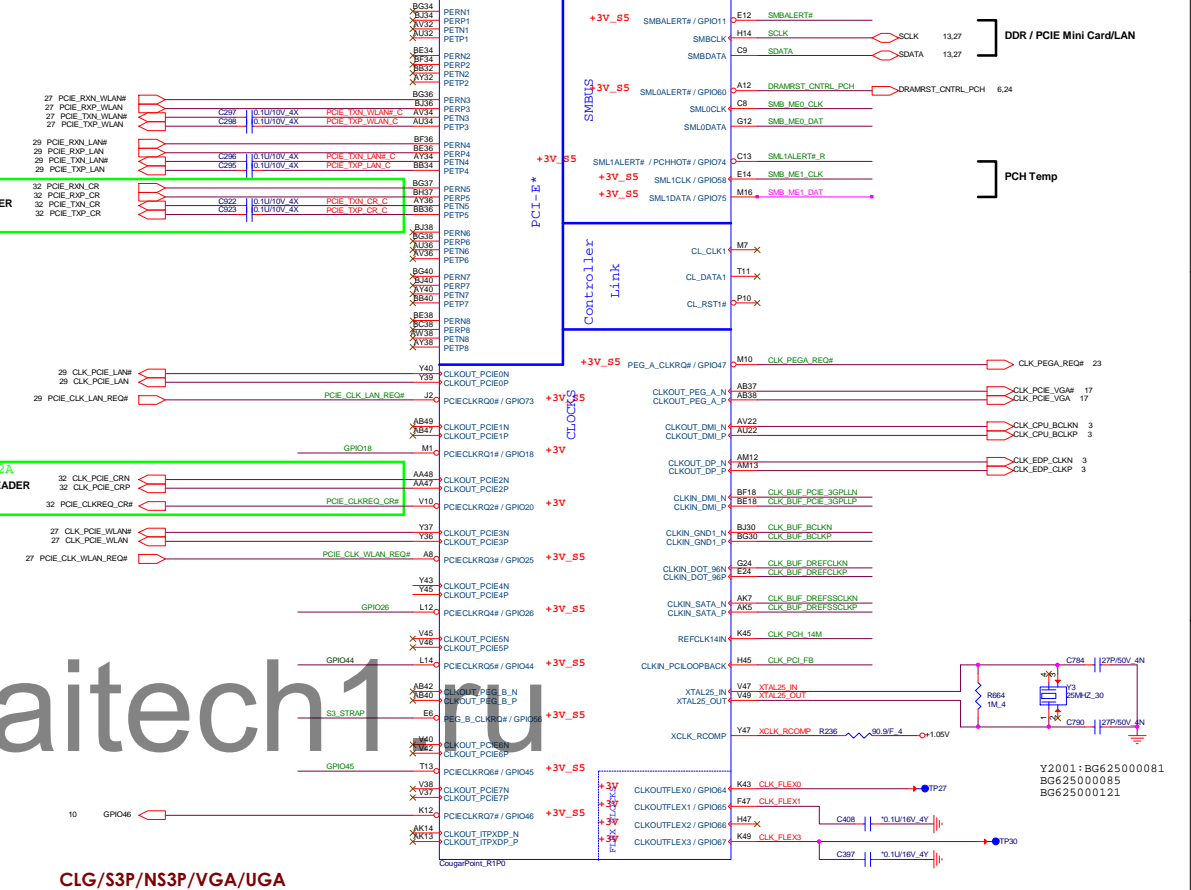
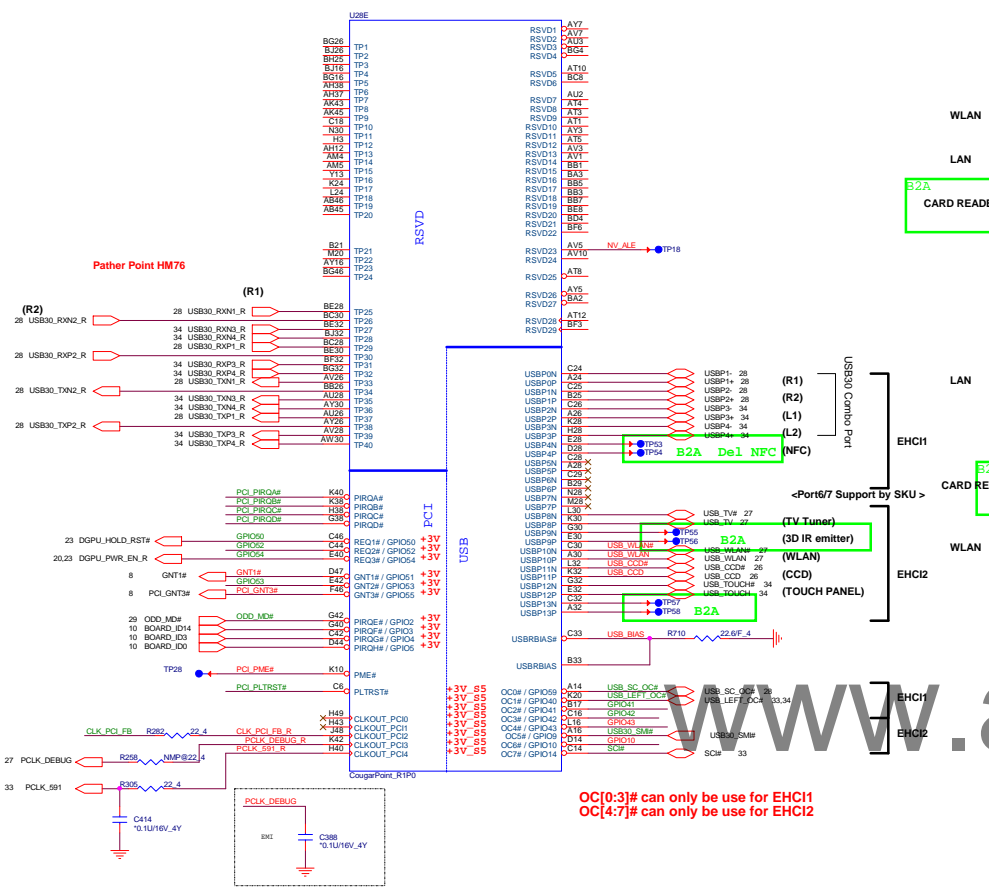


Deep Sx CLG



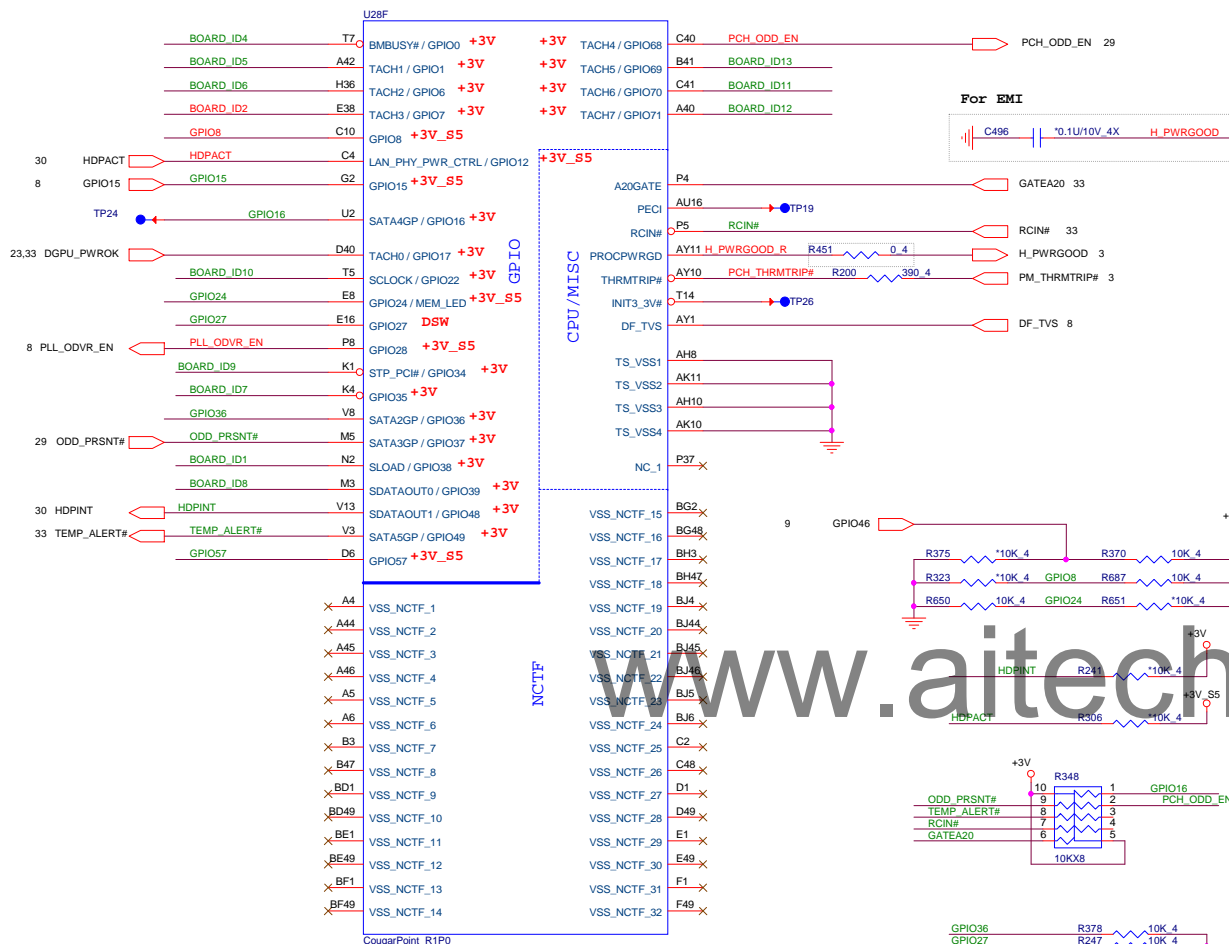
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb, Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Cougar Point-M (PCI,USB,NVRAM) CLG/DEG



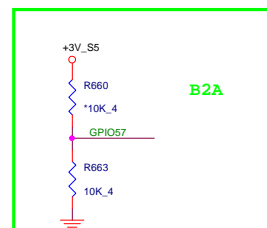
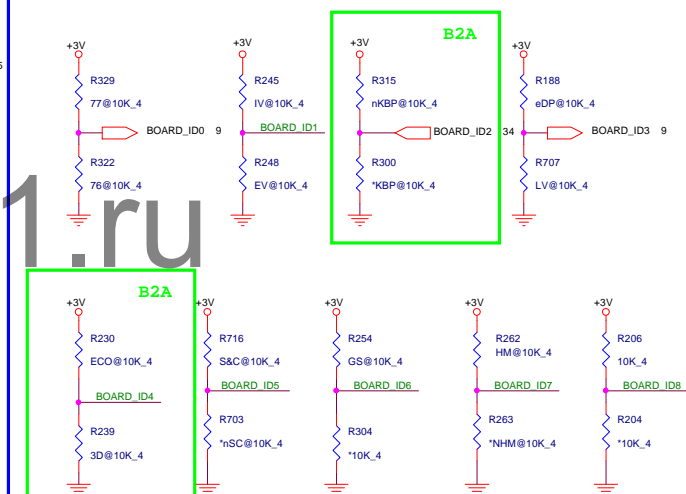
	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

Cougar Point (GPIO,VSS_NCTF,RSVD) CLG

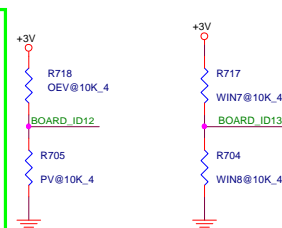


BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

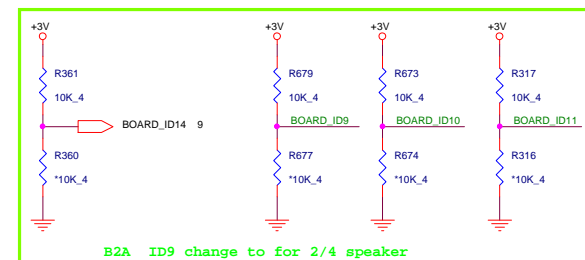
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14
HM77 HM76	H L											
UMA SKU VGA SKU		H L										
W/O LED KB W/ LED KB			H L									
eDP LVDS				H L								
ECO Mode 3D Mode					H L							
S&C Non S&C						H L						
W/ G-sensor W/O G-sensor							H L					
W/ HDMI W/O HDMI								H L				
Premium Gaming									H L			
Only VGA Optimus mode										H L		
WIN7 WIN8											H L	
W/O TV W/ TV												H L



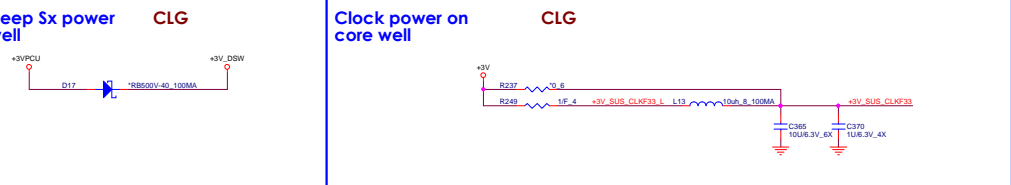
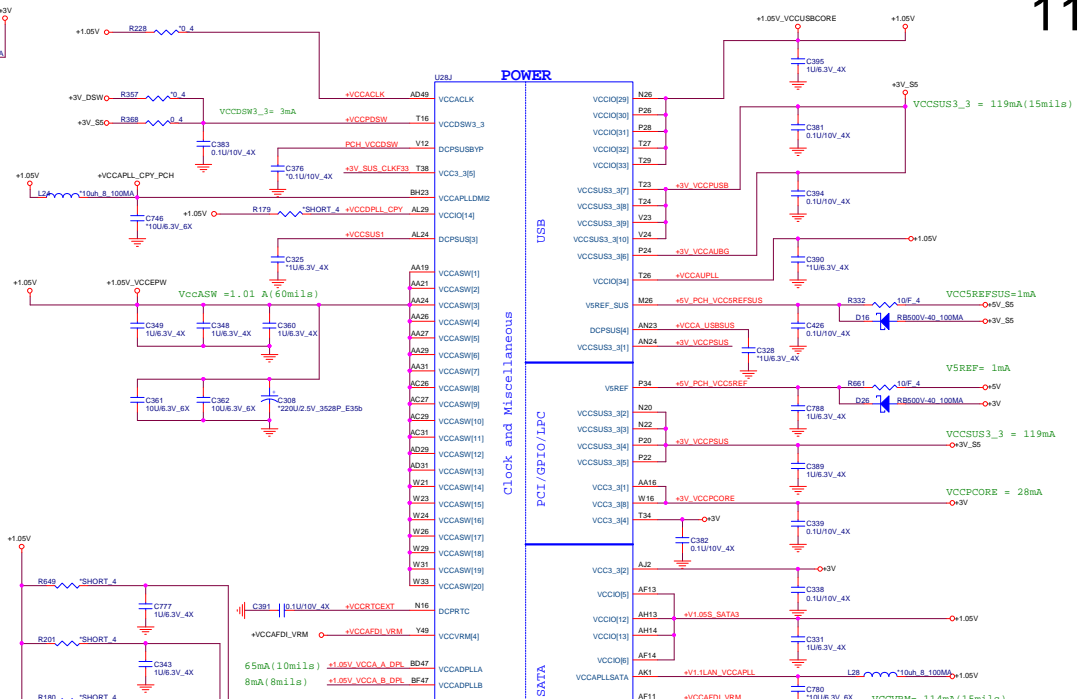
	GPIO57
1000MHz	H
900MHz	L

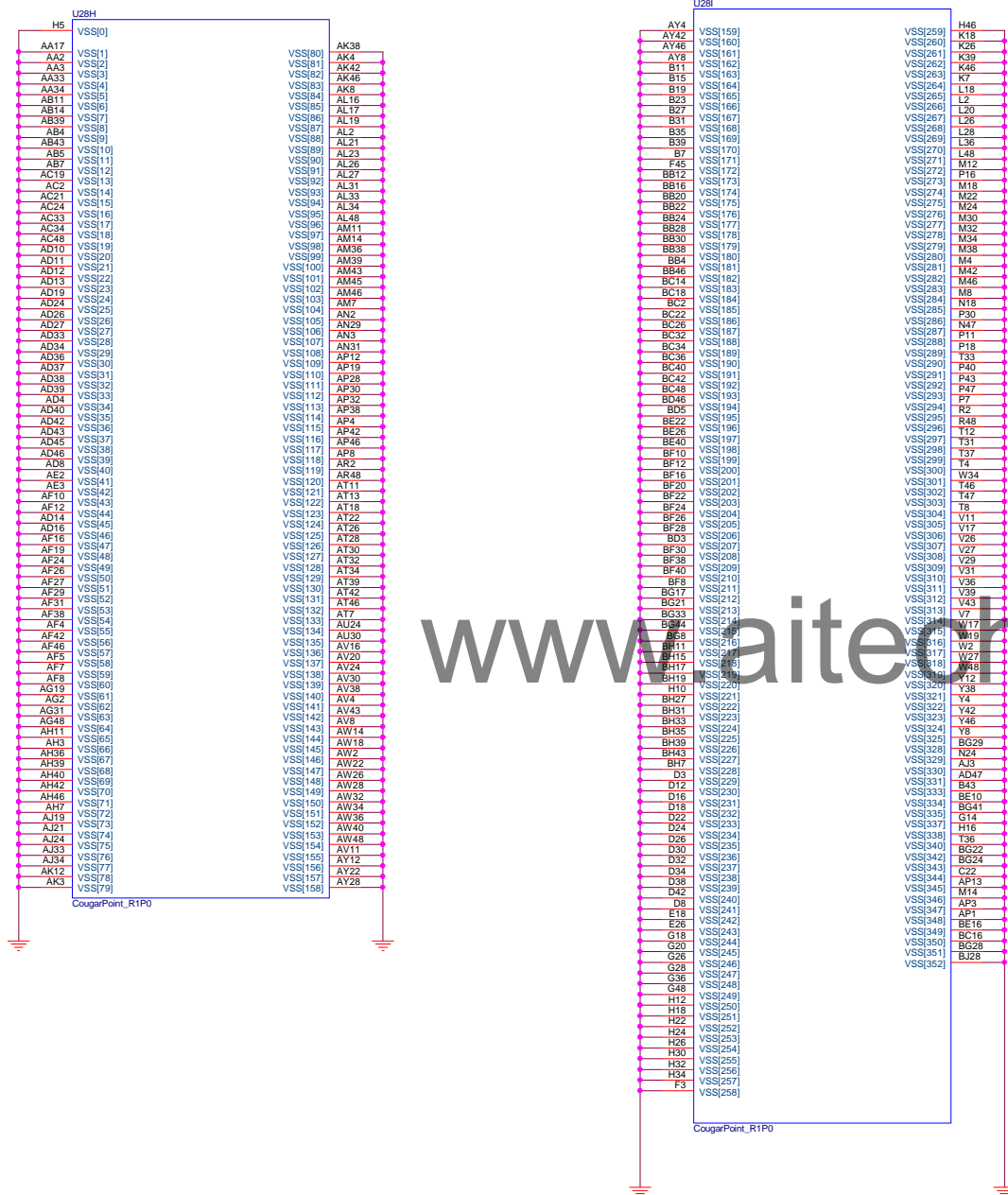


Board ID	ID9	ID10	ID11
4 Speaker	H		
2 Speaker	L		
W/O CIR		H	
W/ CIR		L	
W/O TouchSCN			H
W/ TouchSCN			L



B2A ID9 change to for 2/4 speaker





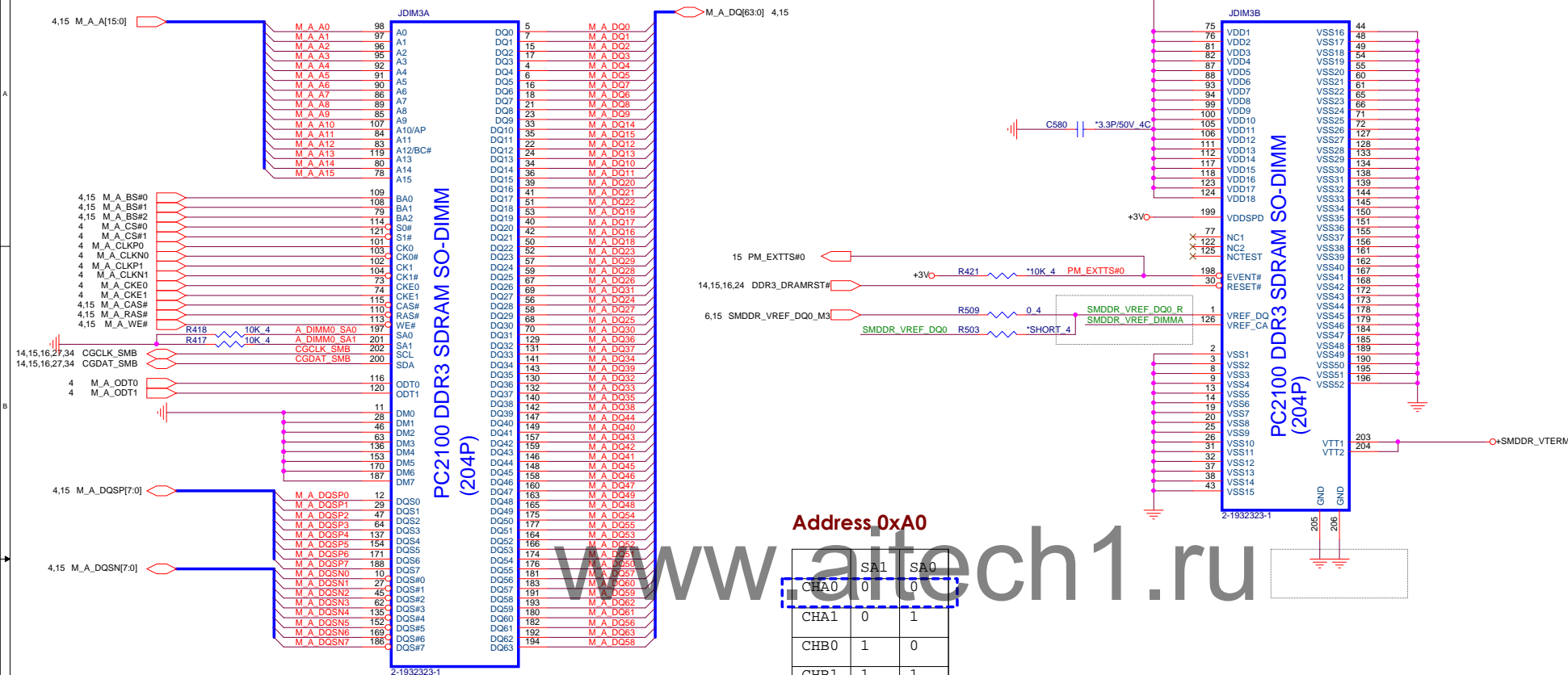
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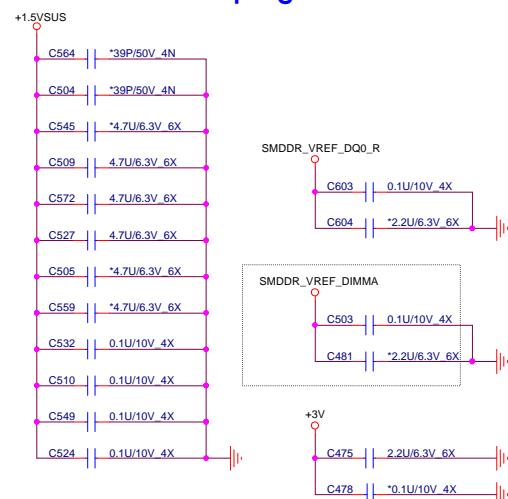
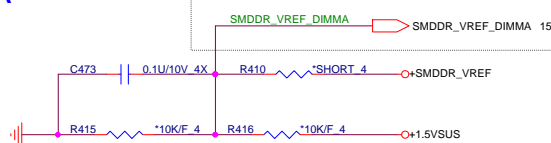
DDR

BOT side close to CPU

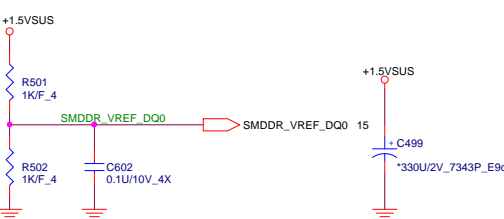
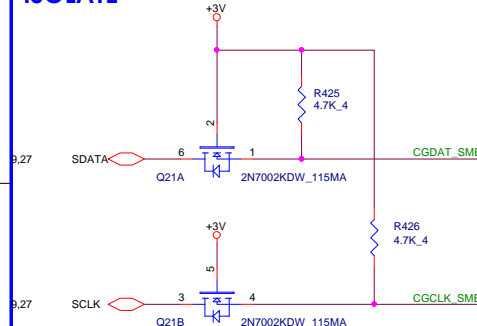
H=8 (Rev)



DDR Power Decoupling DDR

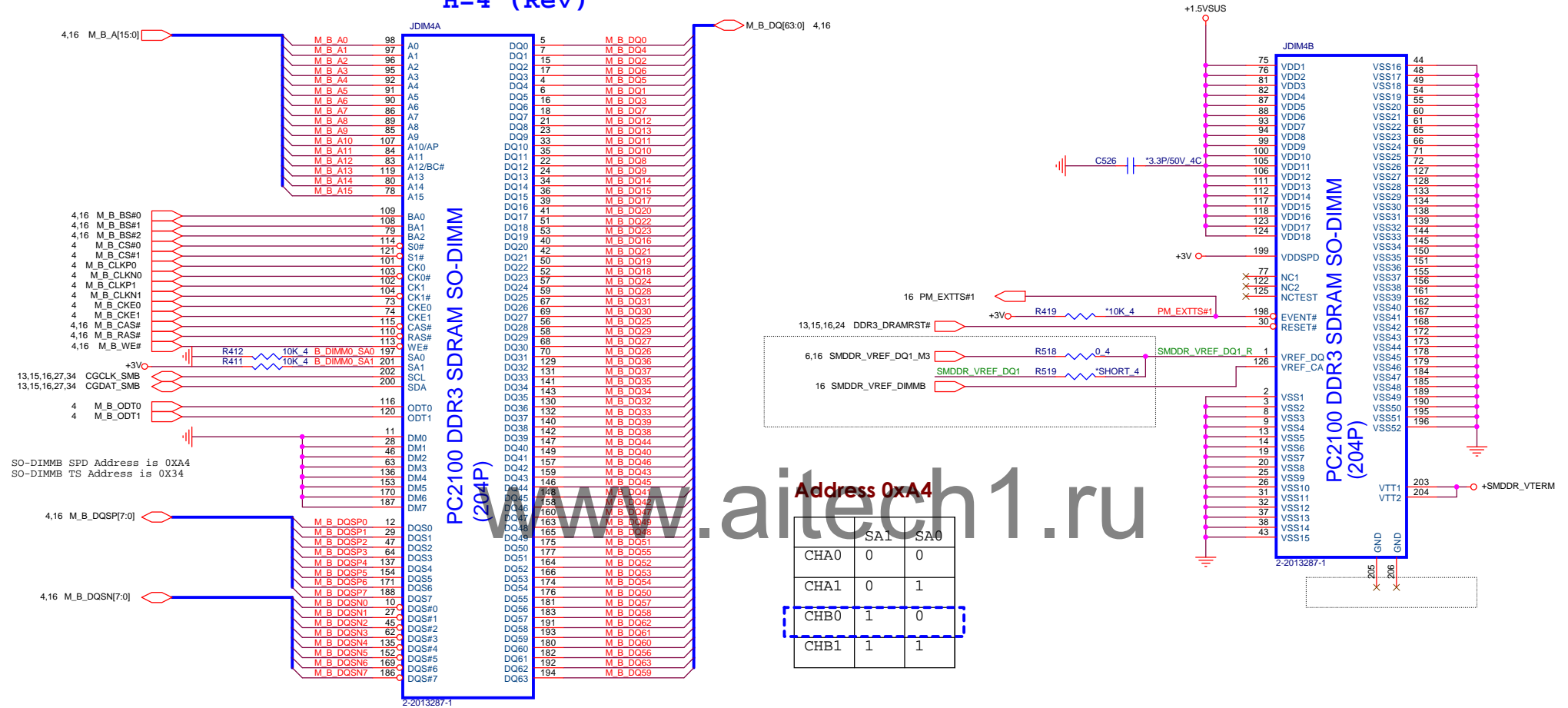
DDR3 VREF DDR
CA

DDR3 VREF DQ (M1) DDR

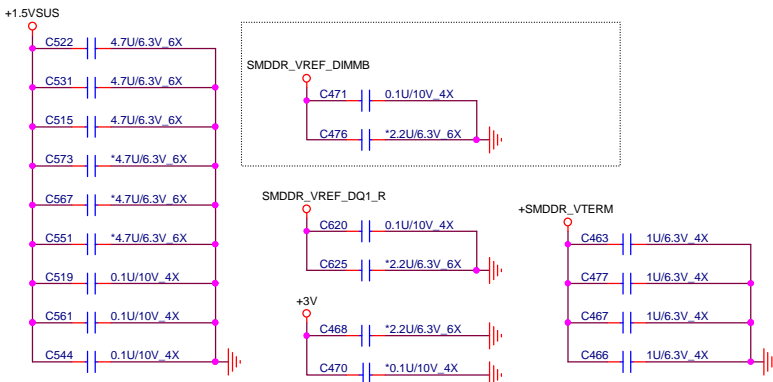
SMBUS
ISOLATE

BOT Side Far Away CPU

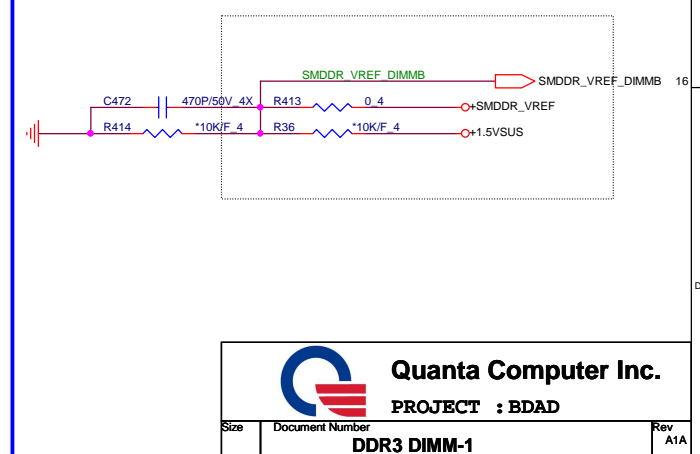
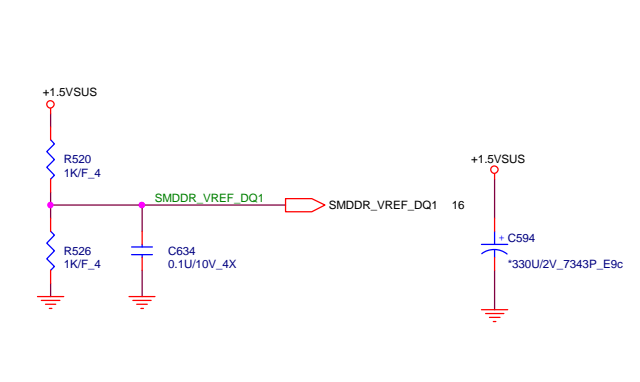
H=4 (Rev)



DDR Power Decoupling DDR



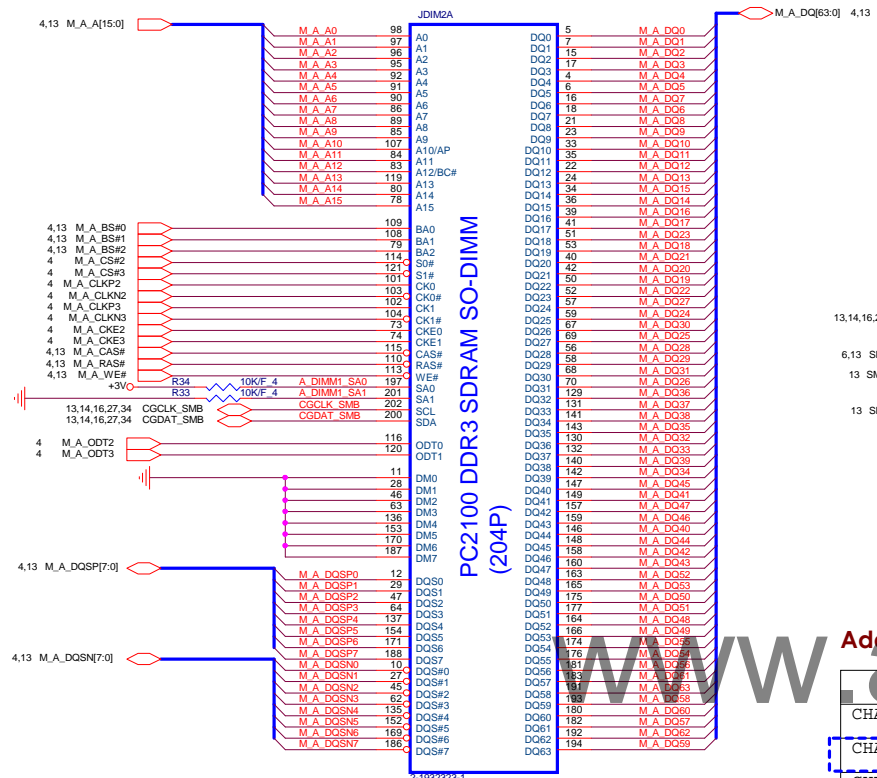
DDR3 VREF DQ (M1) DDR



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TOP side Face to CPU

H=4

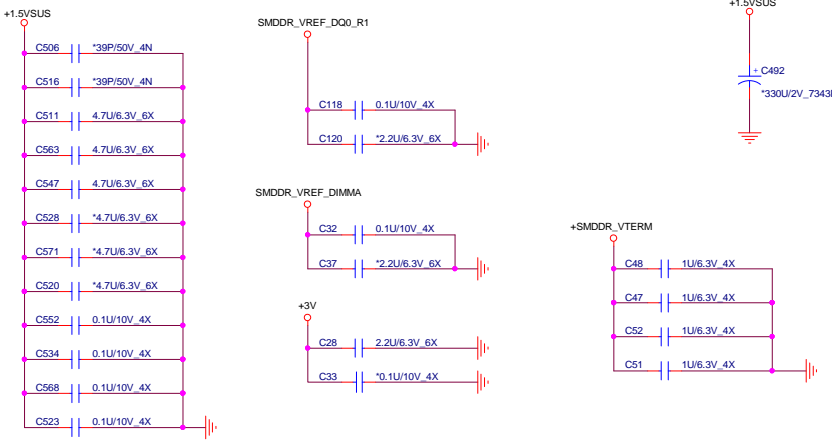


H=4

Address 0xA2

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

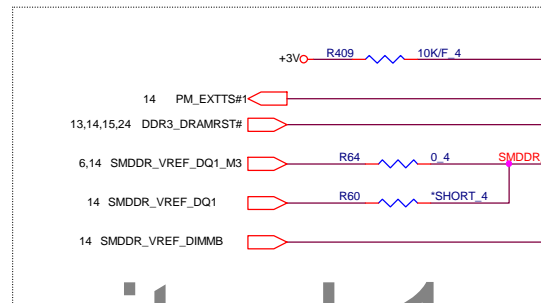
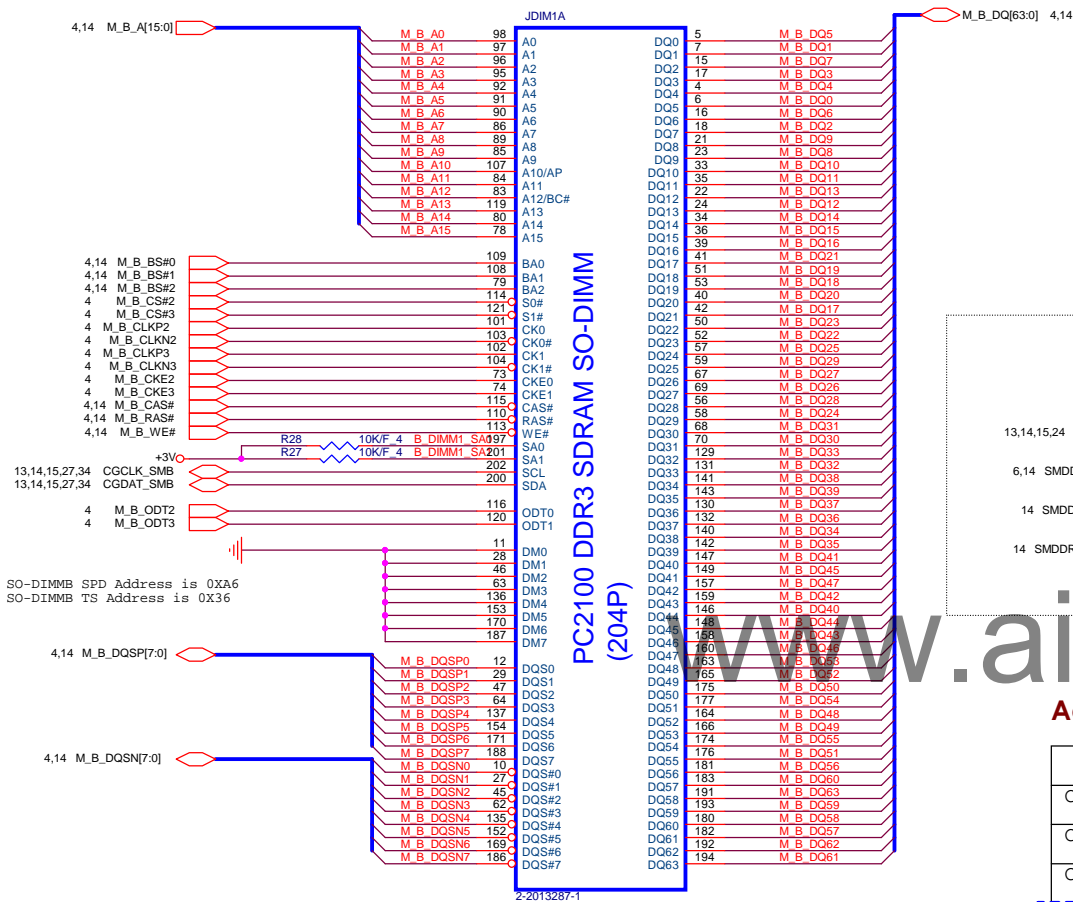
Place these Caps near Memory Down-1



<DDR>

TOP Side Far Away CPU

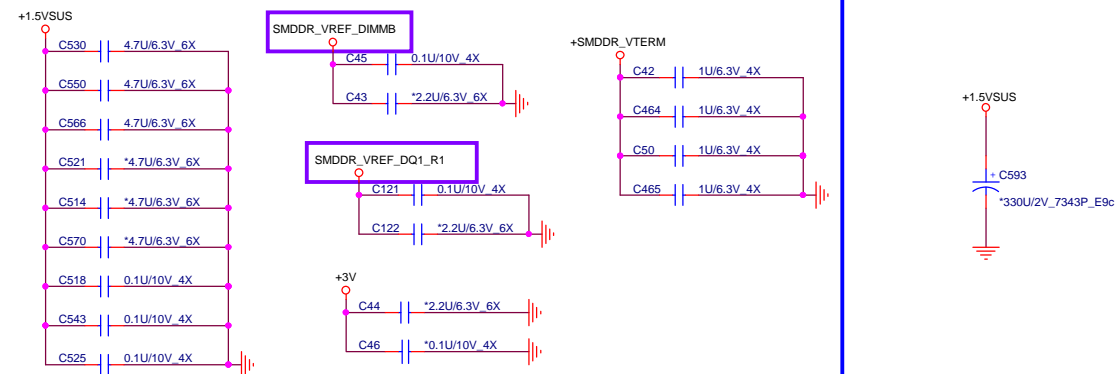
H=4



Address 0xA6

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Place these Caps near So-Dimm1.

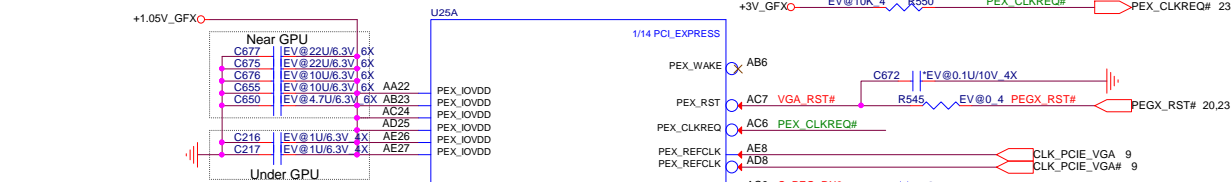


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PROJECT : BDAD

Size	Document Number	Rev
	DDR3 DIMM-1	3B

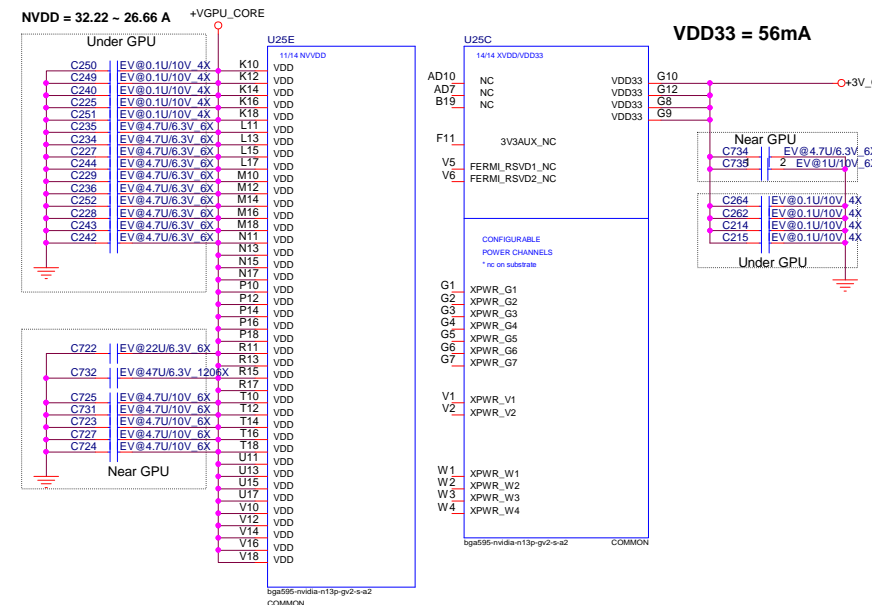
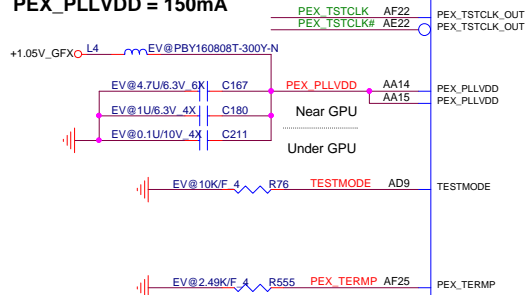
Date: Monday, February 04, 2013 Sheet 16 of 45



**PEX_PLL HVDD +
PEX_SVDD_3V3 = 210mA**



PEX_PLLVDD = 150mA



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**Power up
sequence**

VDD33

+3V_GFX

IFPx_IOVDD

+3V_GFX

NVDD

+VGPU_CORE

FBVDDQ

+1.5V_GFX

PEX_VDD

+1.05V_GFX

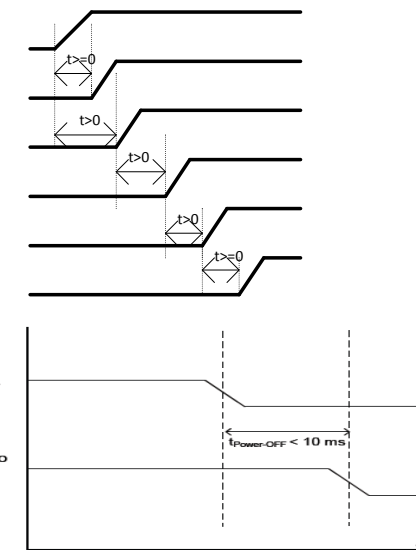
IFPy_IOVDD

+1.05V_GFX

**Power down
sequence**

First Rail to
Power Down

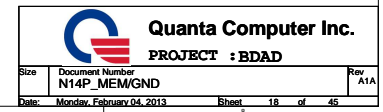
Last Rail to
Power Down

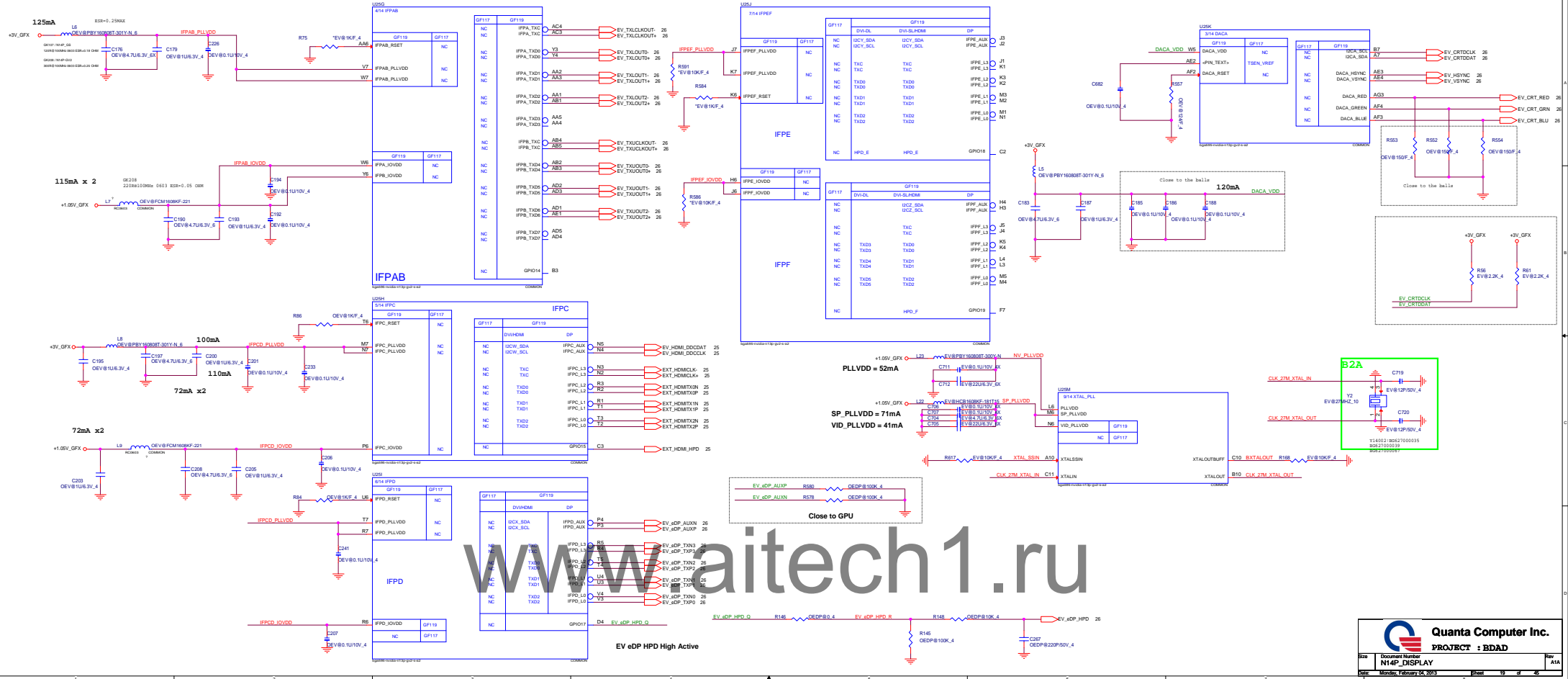


Quanta Computer Inc.

PROJECT : BDAD

Size	Document Number	Rev
	N14P_PEG/NVDD	A1A
Date:	Monday, February 04, 2013	Sheet 17 of 45





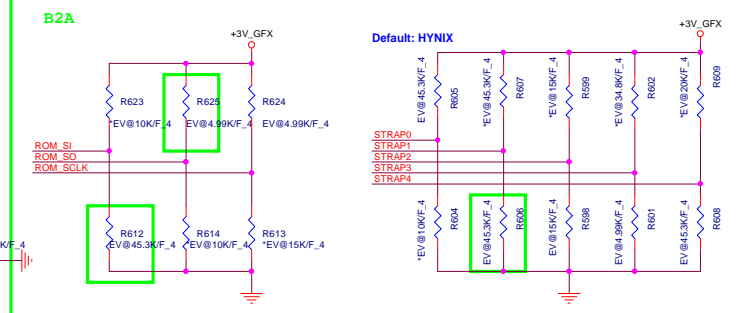
DDR3 Memory TYPE

Vendor	Vendor P/N	QC1 P/N	Size	Max Speed CLK	ROM_SI
Samsung	K4W2G1646E-BC1A (128M*16)	0x7	2GB	1000MHZ	PD 45K
	K4W2G1646E-BC11 (128M*16)	0x7	2GB	900MHZ	PD 45K
	K4W4G1646B-HC11 (256M*16)	0x3	4GB	900MHZ	PD 20K
Micron	MT41J128M16JT-093G:K (128M*16)	0x5	2GB	1000MHZ	PD 30K
	MT41J128M16JT-107G:K (128M*16)	0x5	2GB	900MHZ	PD 30K
	MT41K256M16HA-107G:E (256M*16)	0x1	4GB	900MHZ	PD 10K
Hynix	H5TQ2G63DFR-N0C (128M*16)	0x6	2GB	1000MHZ	PD 35K
	H5TQ2G63DFR-11C (128M*16)	0x6	2GB	900MHZ	PD 35K

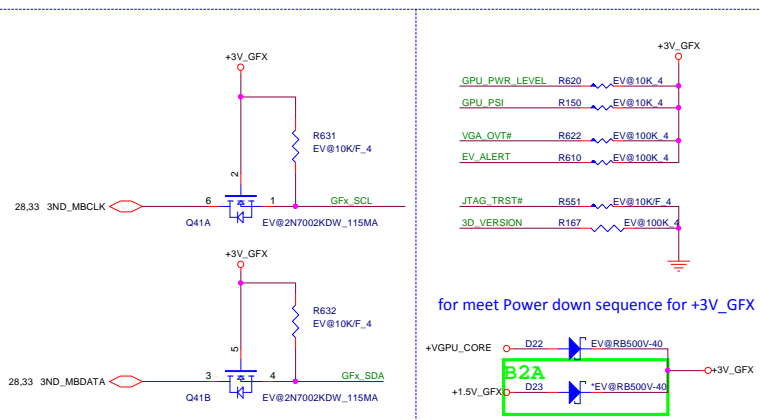
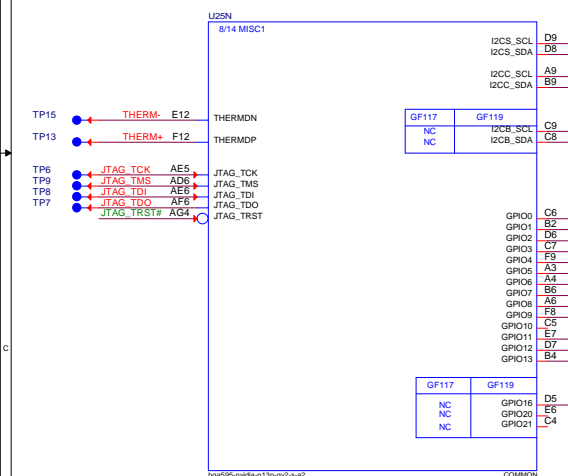
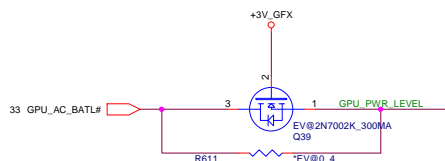
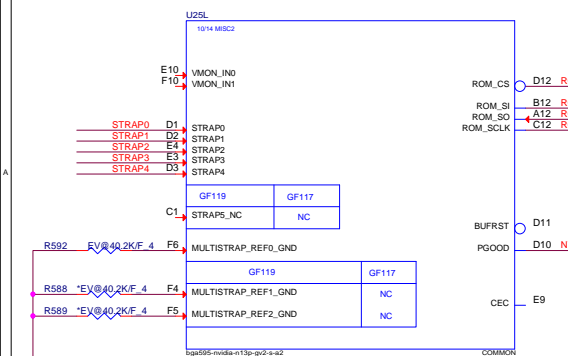
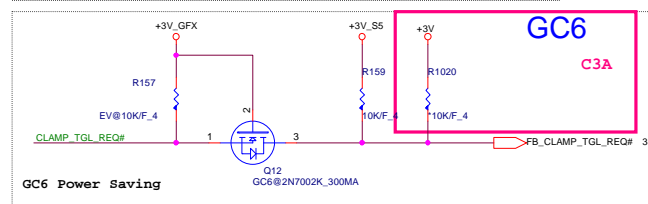
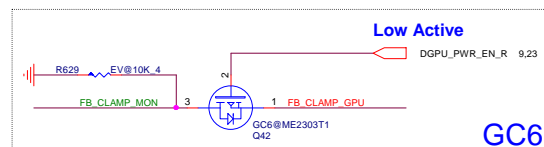
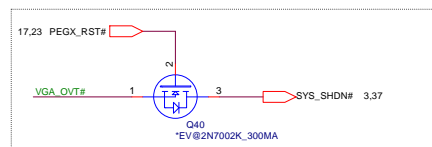
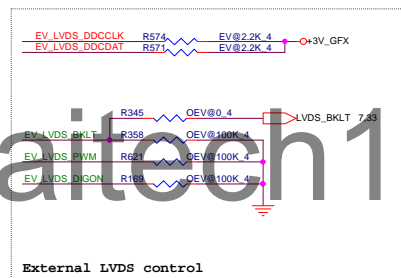
4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB26 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB26 RES CHIP 20K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 36.8K/F 4: CS33482FB22 RES CHIP 36.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

GPIO ASSIGNMENTS

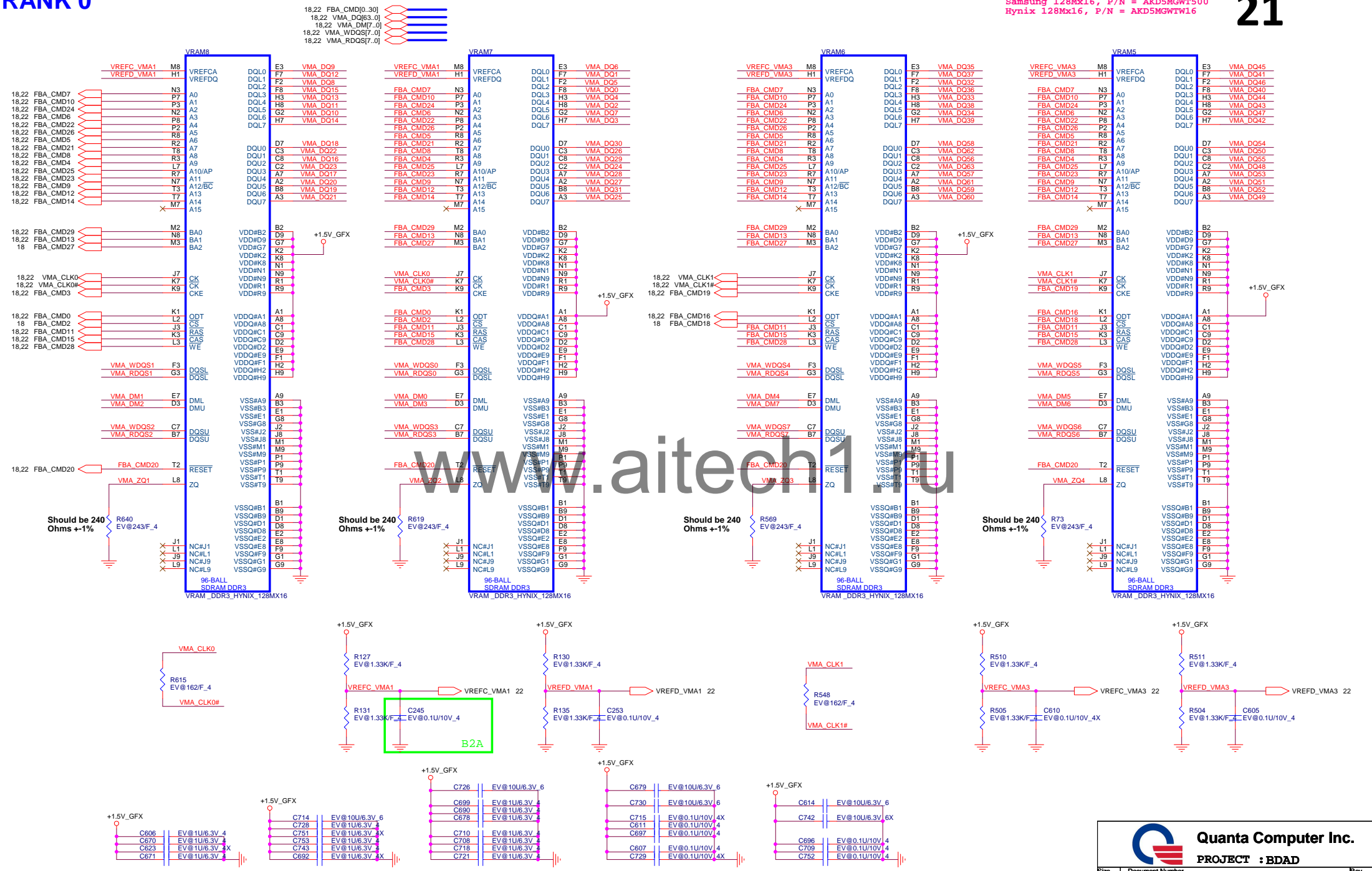
GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

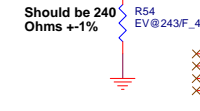


Netname	N14P-GV2	ID:
ROM_SO	10K PU	5kohm PU for Optimus, 10K PU for Discrete
ROM_SCLK	5K PU	0x1000, 0x8, 4.99kohm pull up
STRAP0	45K PU	user strap, 0xF, 45kohm pull up
STRAP1	5K PD	5K PD for QS, 45K PD for after QS
STRAP2	15K PD	Device_ID, 0x0010_15K pull down
STRAP3	5K PD	0x0 for optimus, 5k PD, 0010 for Discrete, 15K PD
STRAP4	45K PD	0x111, 45kohm pull down

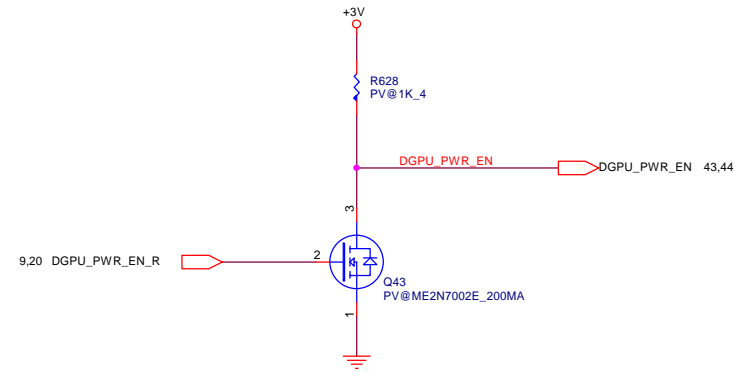


900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16

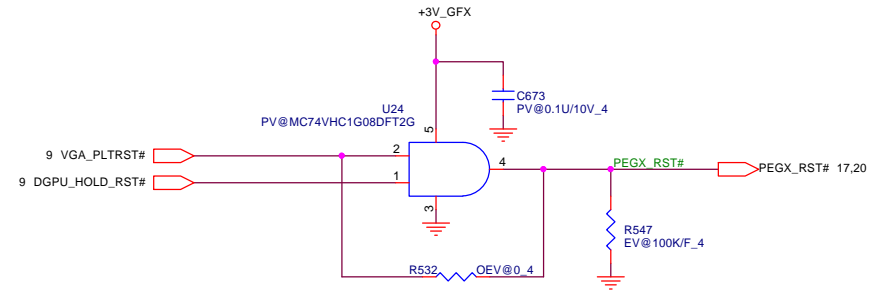




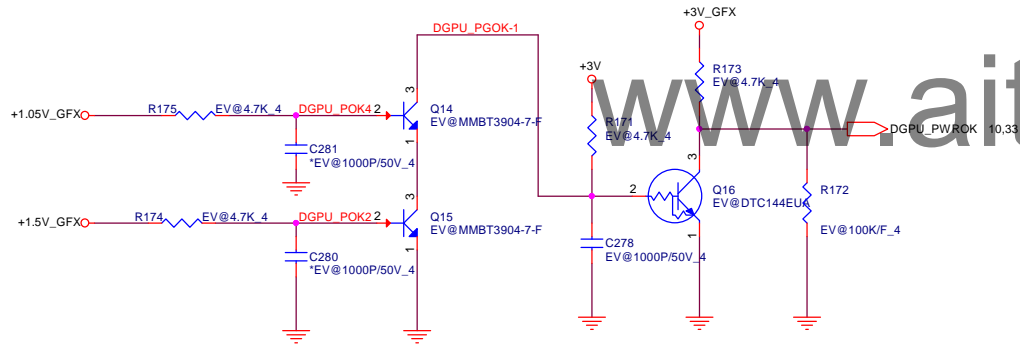
VGA Power Enable Reverse
(Intel --> Low Active)



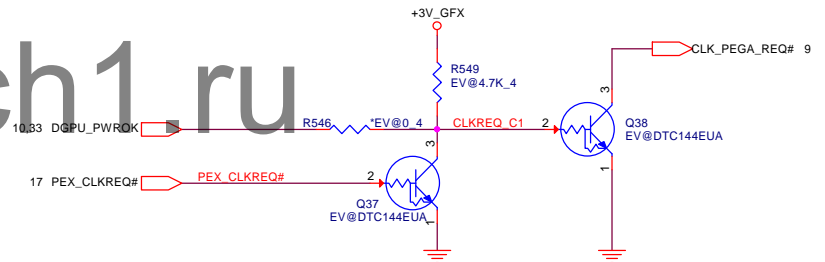
Platform Reset



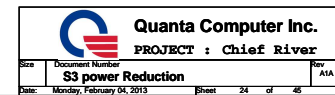
GPU Power Good



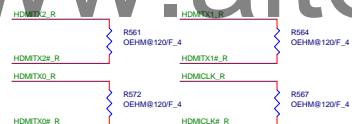
GPU CLOCK REQ



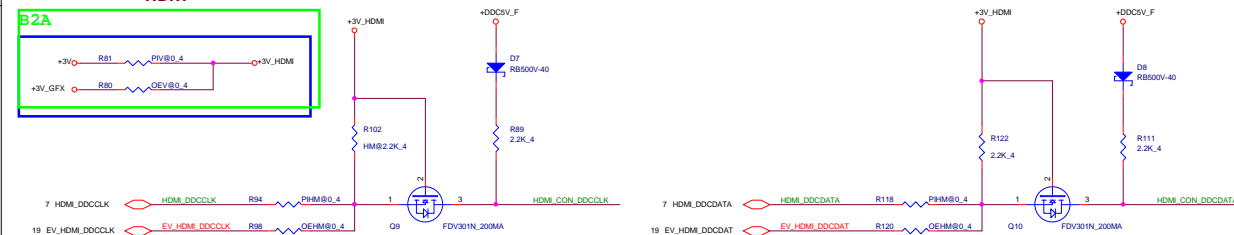
24

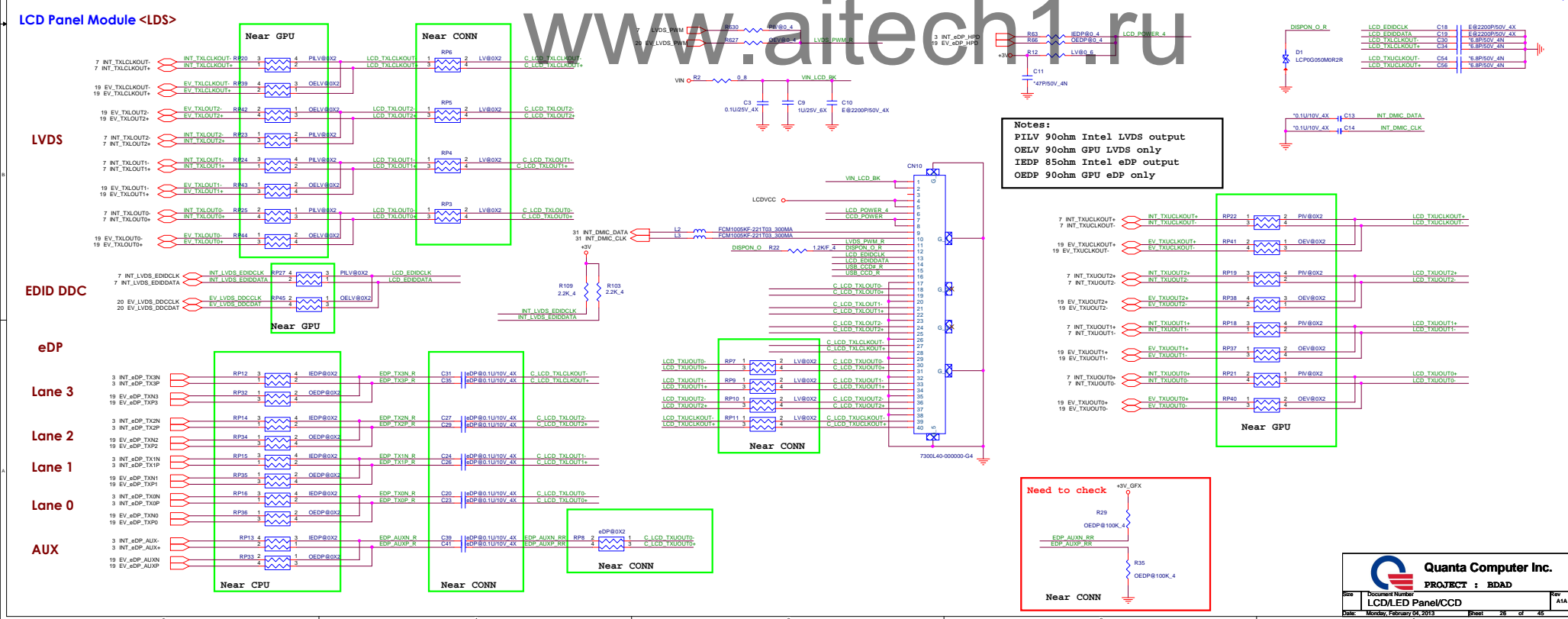
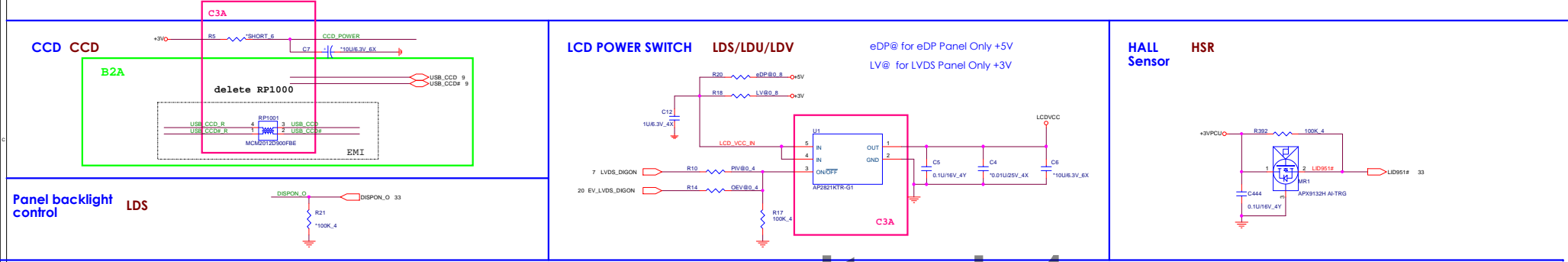
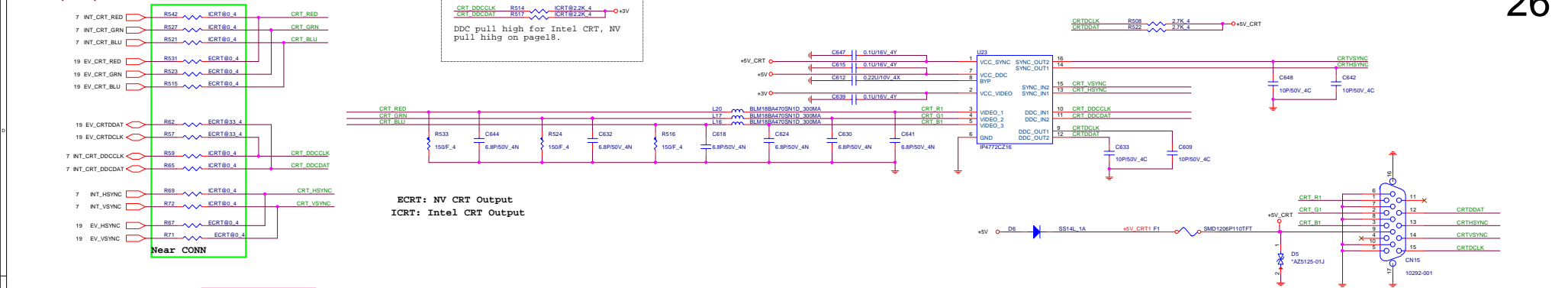


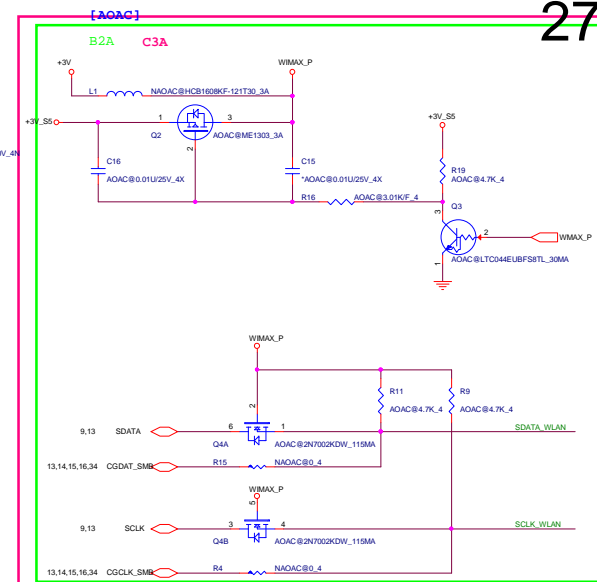
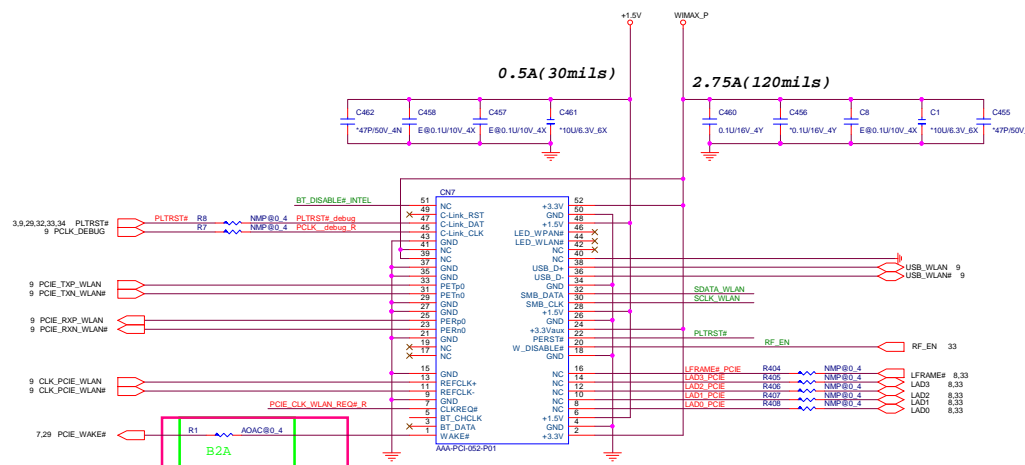
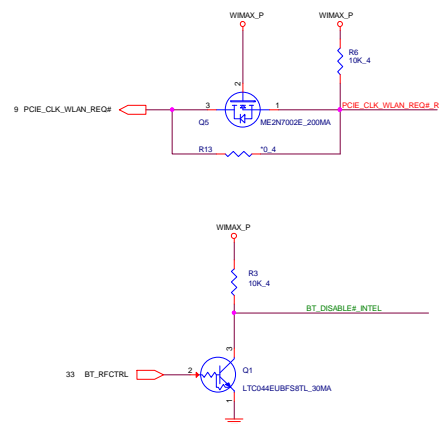
Pin	Signal	Connector	Pin	Signal	Connector	Pin	Signal	Connector
7	IV_HDMTX2	IV_HDMTX2	C685	PHM80_1U10V_4X	PHM80_1U10V_4X		HDMTX2_R	HDMTX2_R
8	IV_HDMTX2P		C686	PHM80_1U10V_4X			HDMTX2_P	
9	EXT_HDMTX2GN		C689	PHM80_1U10V_4X				
10	EXT_HDMTX2GN	EXT_HDMTX2GN	C689	PHM80_1U10V_4X				
7	IV_HDMTX1	IV_HDMTX1	C689	PHM80_1U10V_4X	PHM80_1U10V_4X		HDMTX1_R	HDMTX1_R
8	IV_HDMTX1P		C691	PHM80_1U10V_4X			HDMTX1_P	
9	EXT_HDMTX1P		C694	PHM80_1U10V_4X				
10	EXT_HDMTX1GN	EXT_HDMTX1GN	C694	PHM80_1U10V_4X				
7	IV_HDMTX0	IV_HDMTX0	C701	PHM80_1U10V_4X	PHM80_1U10V_4X		HDMTX0_R	HDMTX0_R
8	IV_HDMTX0P		C702	PHM80_1U10V_4X			HDMTX0_P	
9	EXT_HDMTX0P		C704	PHM80_1U10V_4X				
10	EXT_HDMTX0GN	EXT_HDMTX0GN	C704	PHM80_1U10V_4X				
7	IV_HDMCLK	IV_HDMCLK	C694	PHM80_1U10V_4X	PHM80_1U10V_4X		HDMCLK_R	HDMCLK_R
8	IV_HDMCLKP		C695	PHM80_1U10V_4X			HDMCLK_P	
9	EXT_HDMCLKP		C697	PHM80_1U10V_4X				
10	EXT_HDMCLKGN	EXT_HDMCLKGN	C697	PHM80_1U10V_4X				



HDMI-SMBus <HDM>





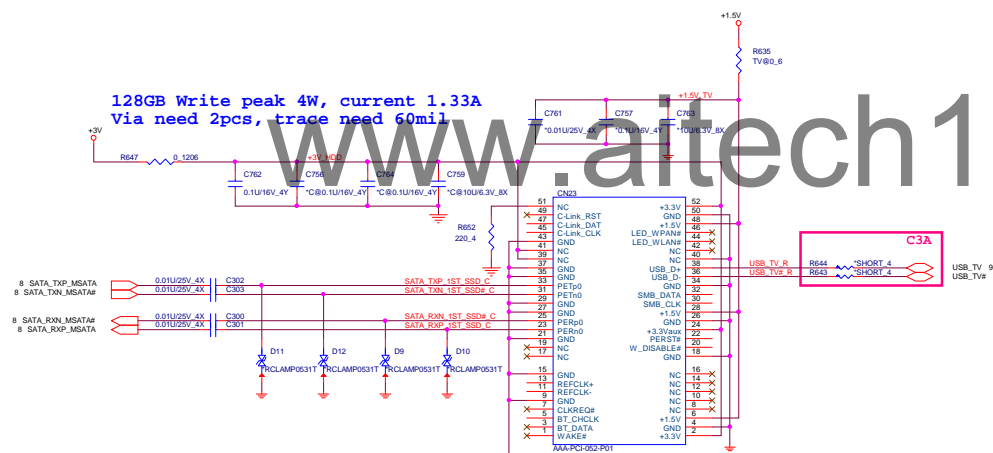


TV Tuner / MSATA

<SSD>

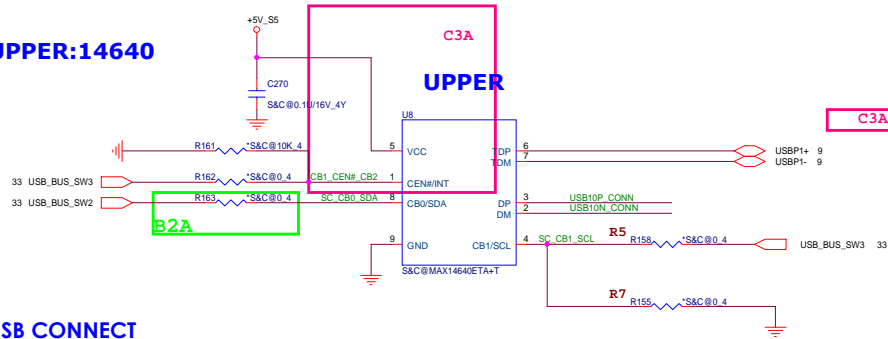
TV Tuner: 1.5V@240mA 3.3V@470mA

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil



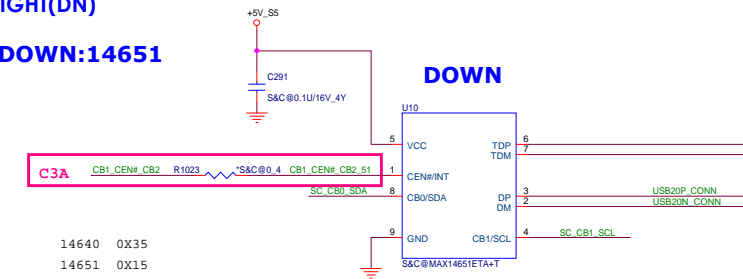
USB CONNECT RIGHT(UR)

UPPER:14640



USB CONNECT RIGHT(DN)

DOWN:14651



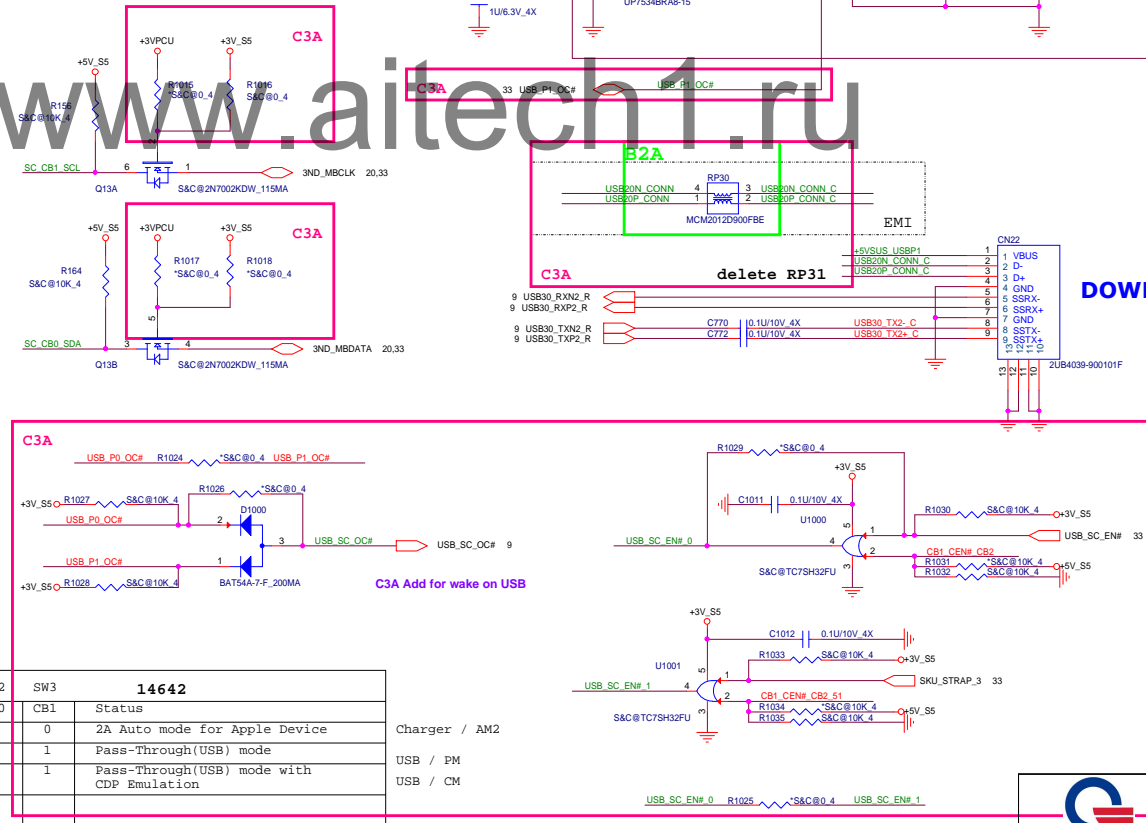
	R1	R2	R3	Q5018	R5	Q5018	R7	R8
14566		V	V		V		V	
14600		V	V		V		V	
14617(with CB2)	V		V		V		V	
14617(no CB2)			V		V		V	
14641/42/44			V		V		V	
14640			V		V		V	

I2C Control			14640/14651		
2	1	0	Status		Charger / AM2
0	0	0	2A Auto mode for Apple Device		USB / PM
0	0	1	Pass-Through(USB) mode		Charger / FM
0	1	0	Force dedicated charger mode		USB / CM
0	1	1	Pass-Through(USB) mode with CDP Emulation		Charger / AM1
1	0	0	1A Auto mode for Apple Device		Charger / AP1
1	0	1	1A Forced mode for Apple Device		Charger / AP2
1	1	0	2A Forced mode for Apple Device		Charger / SS
1	1	1	2A Forced mode for Samsung Device		

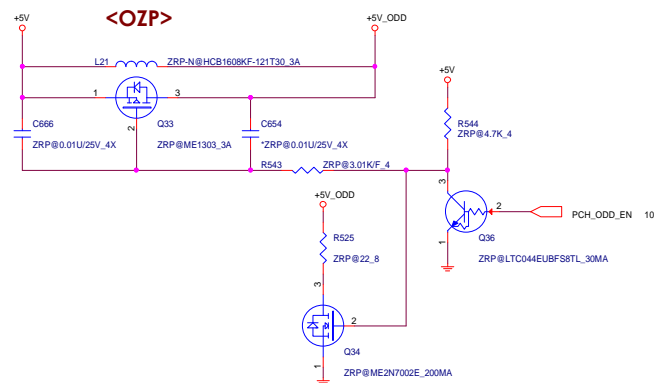
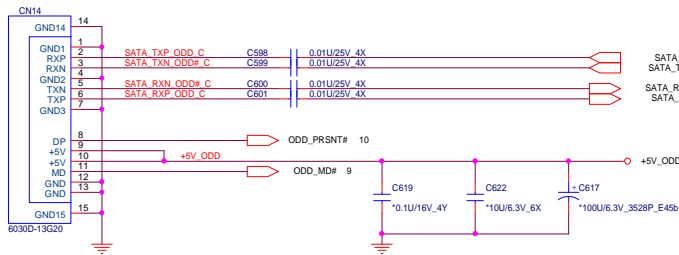
SW2	SW3	14644		
CB0	CB1	Status		Charger / AM2
0	0	2A Auto mode for Apple Device		Charger / FM
1	0	Force dedicated charger mode		USB / PM
0	1	Pass-Through(USB) mode		USB / CM
1	1	Pass-Through(USB) mode with CDP Emulation		

SW2	SW3	14642		
CB0	CB1	Status		Charger / AM2
X	0	2A Auto mode for Apple Device		USB / PM
0	1	Pass-Through(USB) mode		USB / CM
1	1	Pass-Through(USB) mode with CDP Emulation		

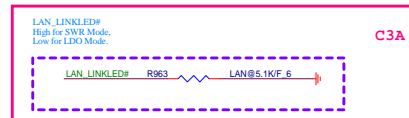
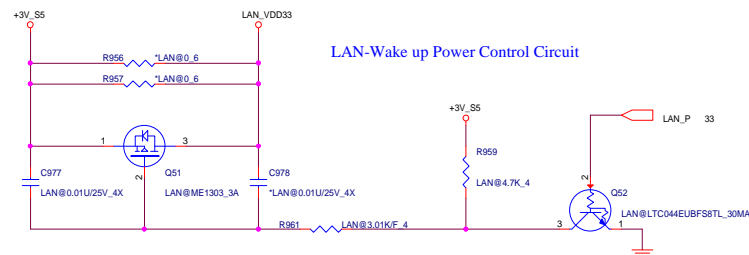
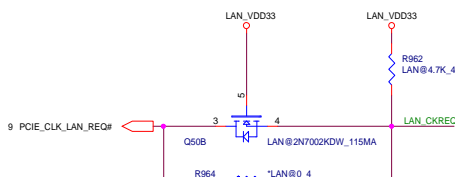
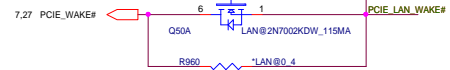
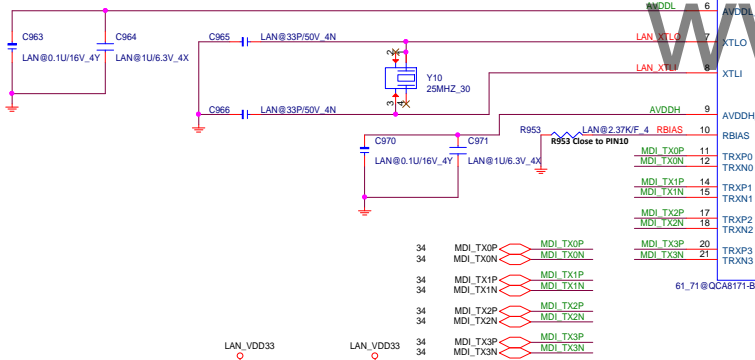
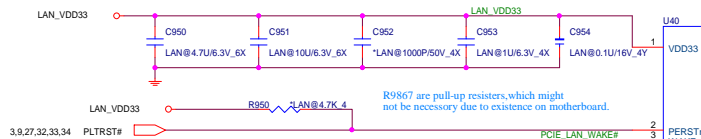
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ODD Zero power .
(Only for Intel)

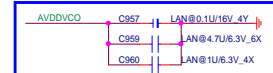


277mA(30mils)

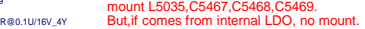


The pin 38 "LED0" doesn't pull down to choose low core voltage. (It's internal pull up) by FAE's command.20120914

AVDDVCO add C957,C959,C960 by FAE's command.20120914



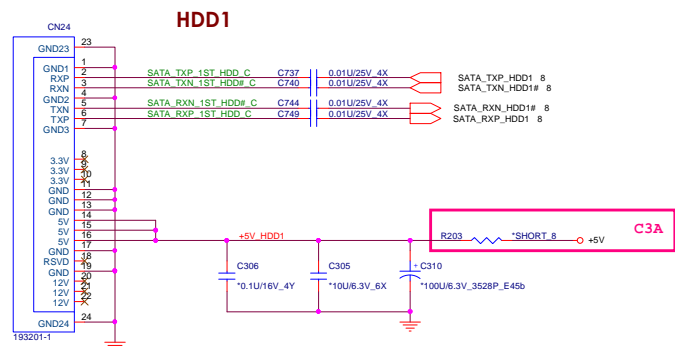
If AVDDL/DVDDL comes from internal SWR:
mount L5035,C5467,C5468,C5469.
But,if comes from internal LDO, no mount.



LED0 = LAN_ACTLED	1	High core voltage.(default = 1)
	0	Low core voltage.
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select
	0	LDO linear regulator select (default = 0)
LED2 = EXTCCLK Use Xtal=>NC	1	25MHz External clock input
	0	48MHz External clock input

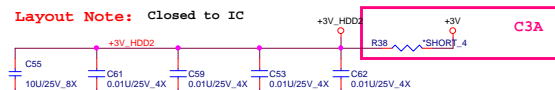
SATA HDD1

HDD1

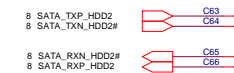


2nd HDD SATA Re-driver

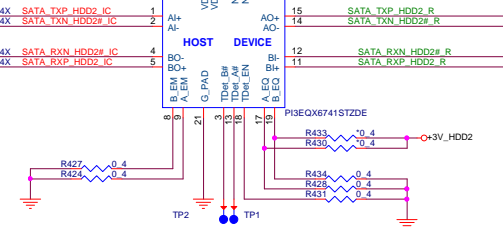
Layout Note: Closed to IC



Connect to PCH side



Connect to HDD connector

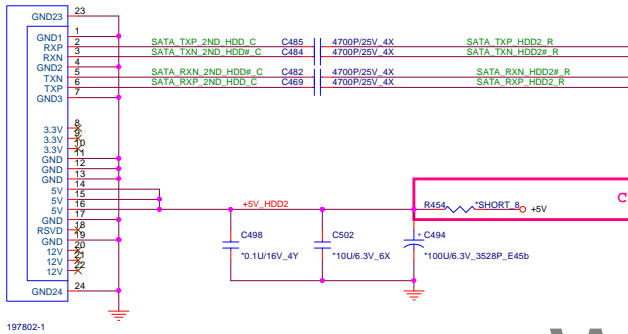


A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

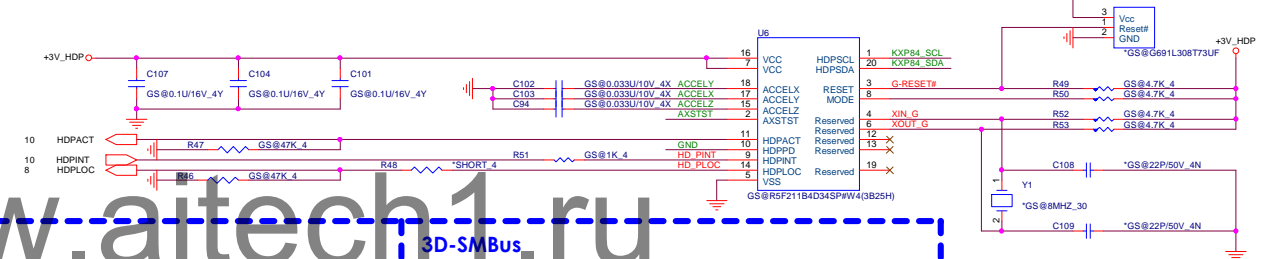
A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

SATA HDD2

HDD2



3D-u-micro P <GSR>

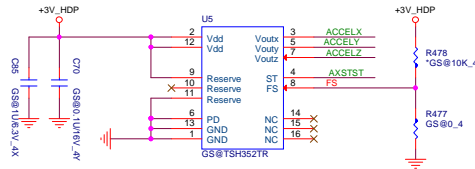
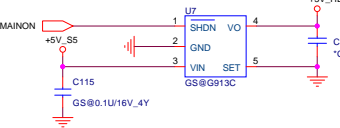


3D-Sensor IC

<GSR>

3D-LDO Power <GSR>

0.3A



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

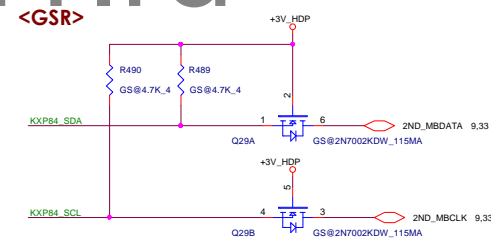
PD	0	1
	Normal Mode	Power-down mode

HDPDP selection

HDPDP	0	1
	Normal Mode	Power-down mode

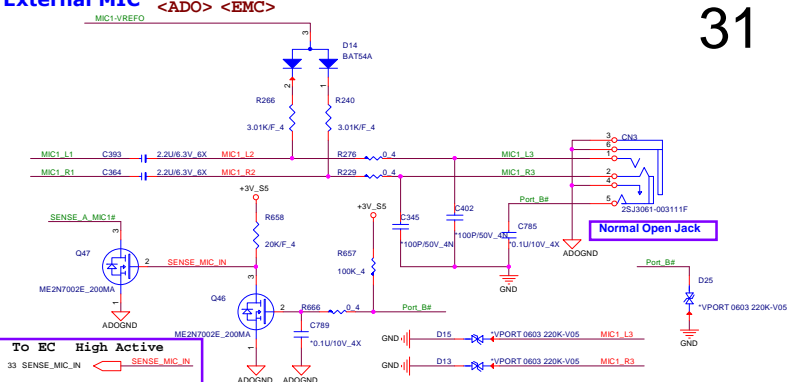
3D-SMBus

<GSR>



Size Document Number
HDD/ODD/G-Sensor

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The diagram shows the B2A module with the following connections:

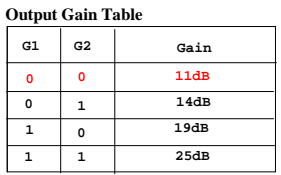
- Inputs:** HP_A_L and HP_A_R are connected to resistors R716 and R701 (5.1K Ω) respectively, which are then connected to HPOUT-L2 and HPOUT-R2.
- Outputs:** HPOUT-L3 and HPOUT-R3 are connected to Port_A# and Port_B# of the 25J3061-003111F connector.
- Power:** C810 and C817 (100pF/50V_4N) are connected to a 0.1uF/16V_4Y capacitor, which is then connected to the ADGND pin of the connector.
- Other Connections:** HPOUT-L3 is also connected to C816 (0.1uF/10V_4X) and HPOUT-R3 is connected to C809 (0.1uF/10V_4X).

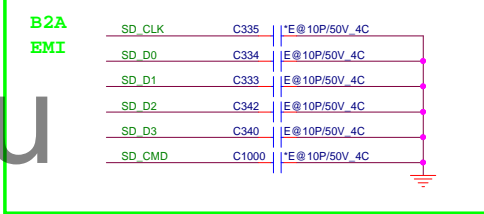
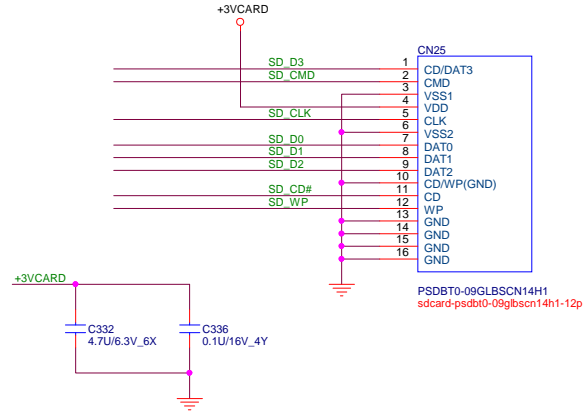
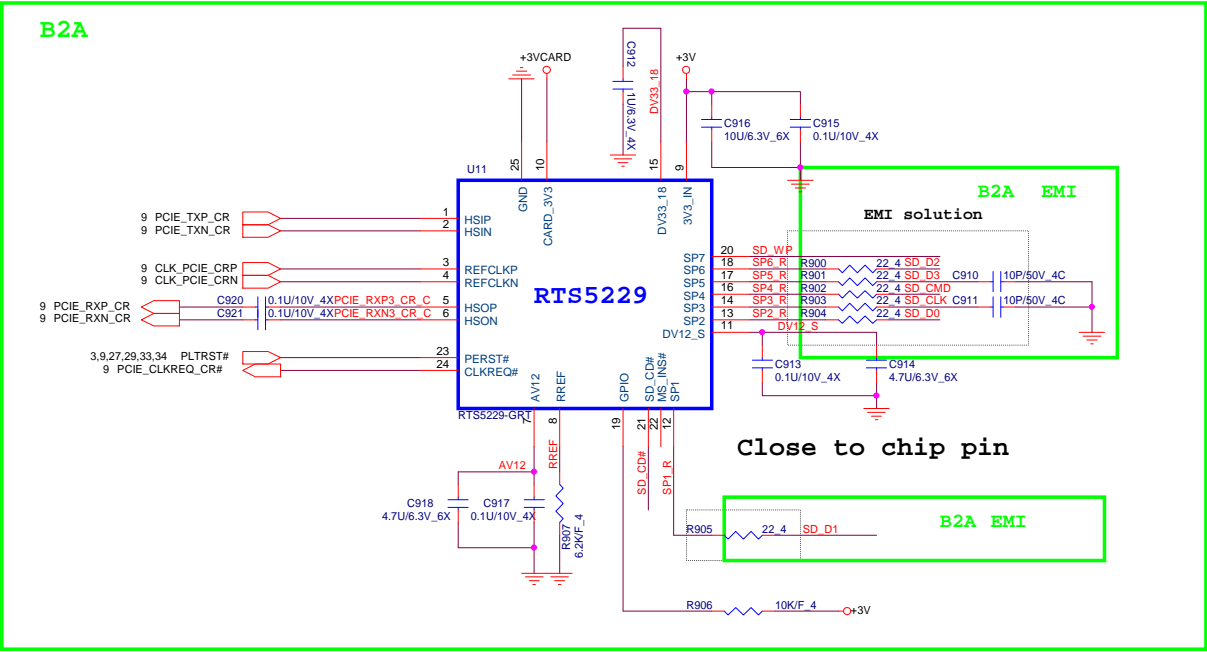
Close to Connector

Pin	Signal
R541	105_SPK_R+
R542	105_SPK_R-
R536	105_SPK_L+
R537	105_SPK_L-

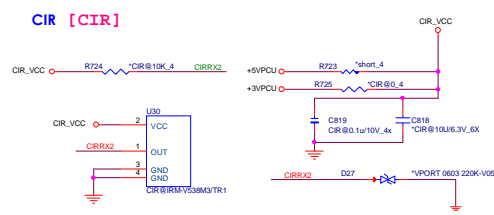
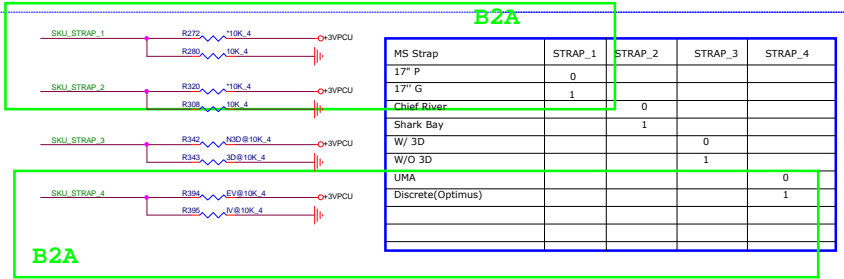
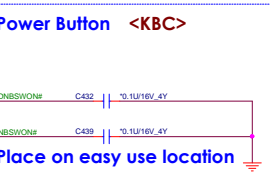
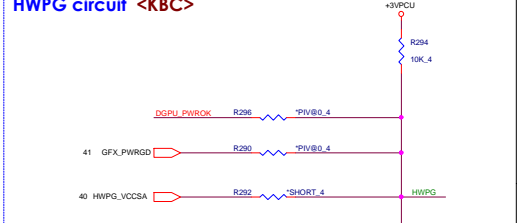
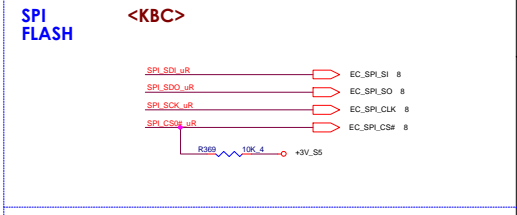
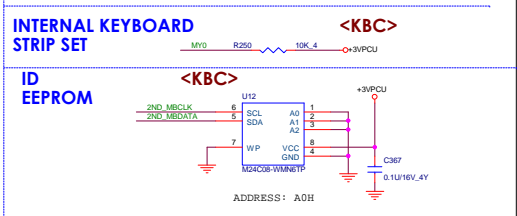
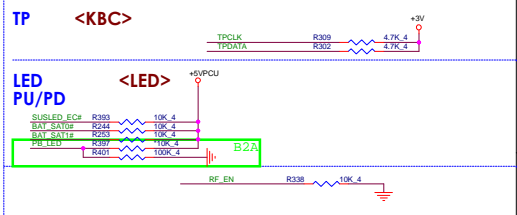
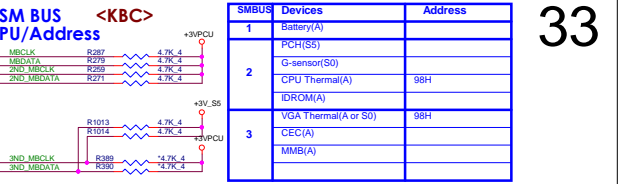
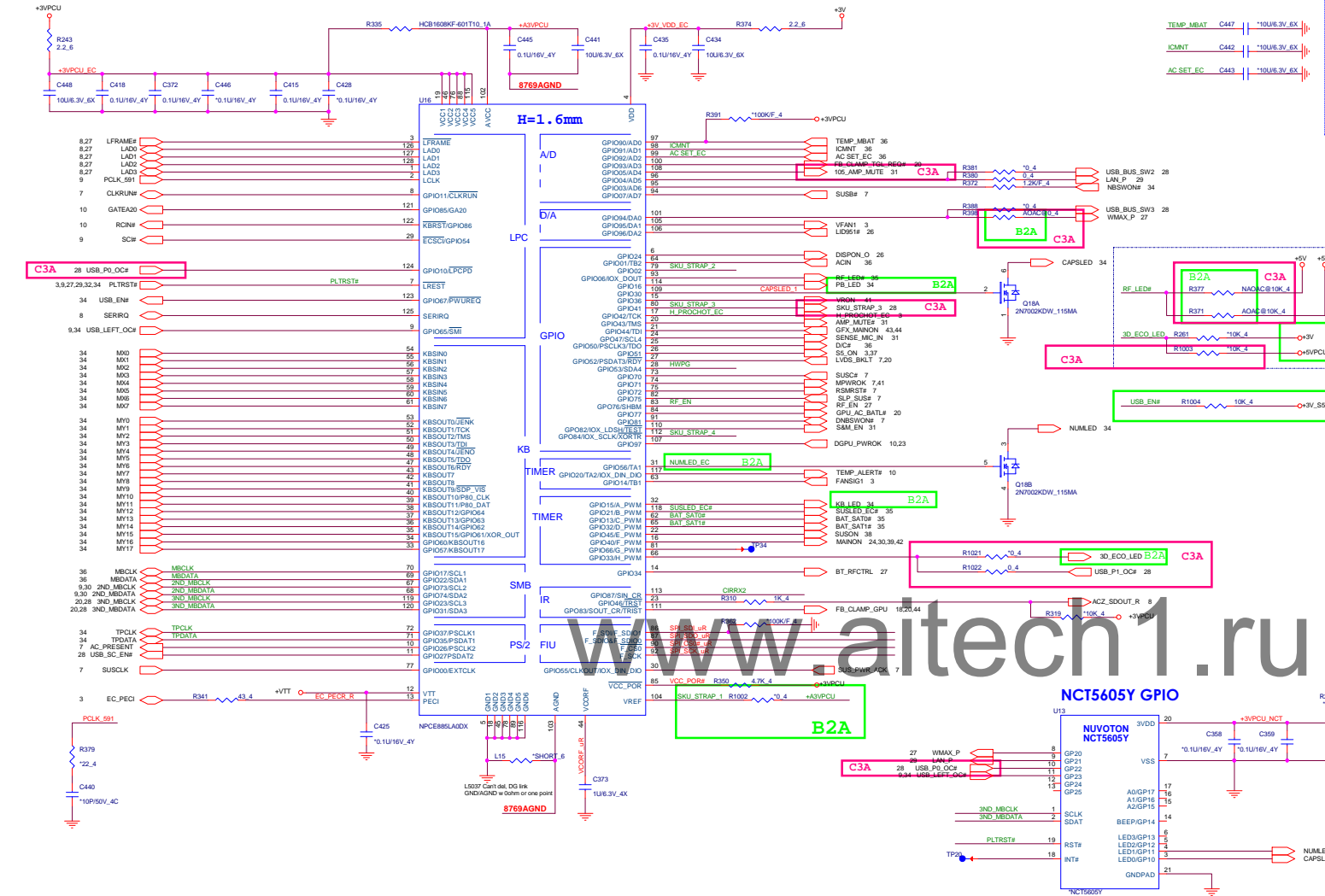
B2A EMI

Ground connection: 88266-08d-0-r

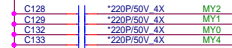
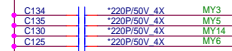
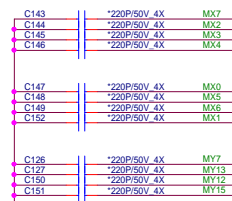




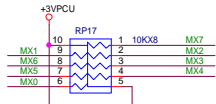
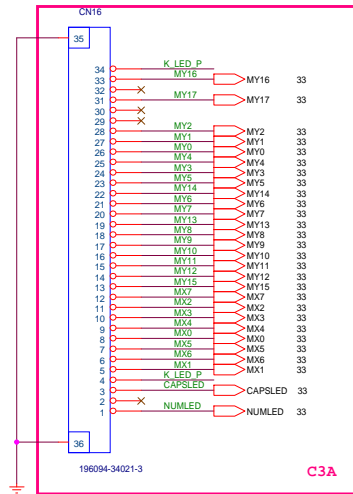
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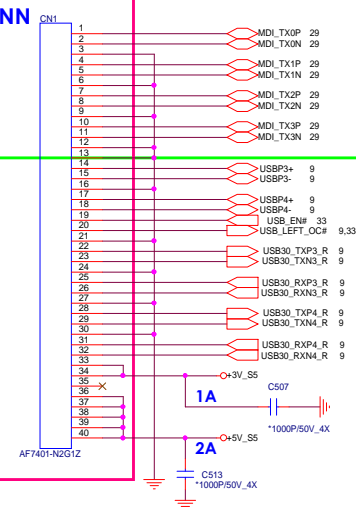
INT Keyboard <KBC>



(10mils)



Daughter Board CONN

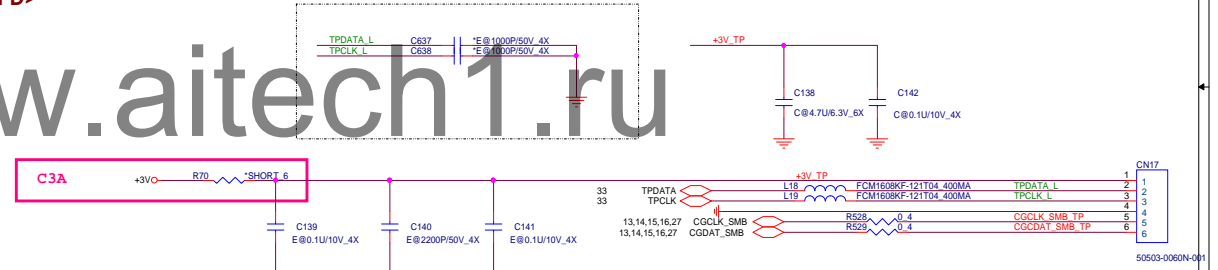
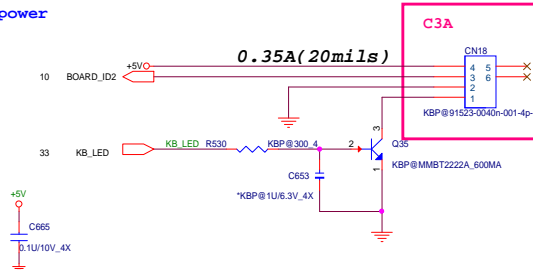


TP board <TPD>

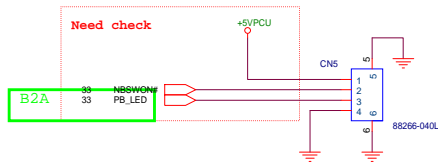
www.aitech1.ru

K/B LED power <KBP>

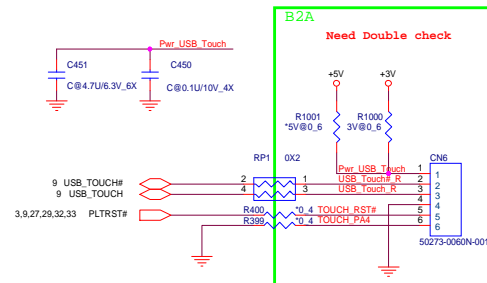
0.35A(20mils)



Power board w LED <PSW>



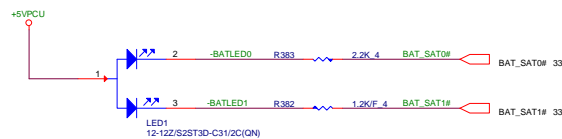
TOUCH PANEL <TPP>



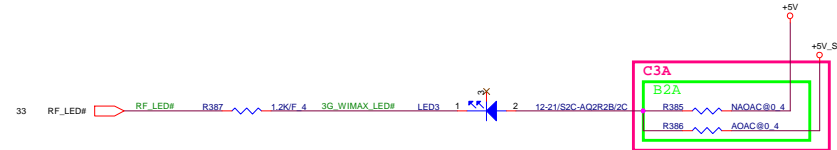
LED LED

BATTERY

BEW00011ZA0



RF LED LED

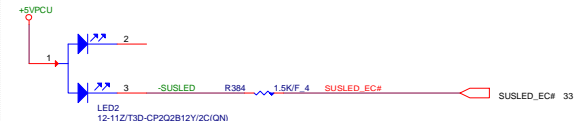


35

POWER LED

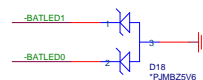
BEWH0139Z00

S0 Mode = White ON
S3 Mode = White BLINK

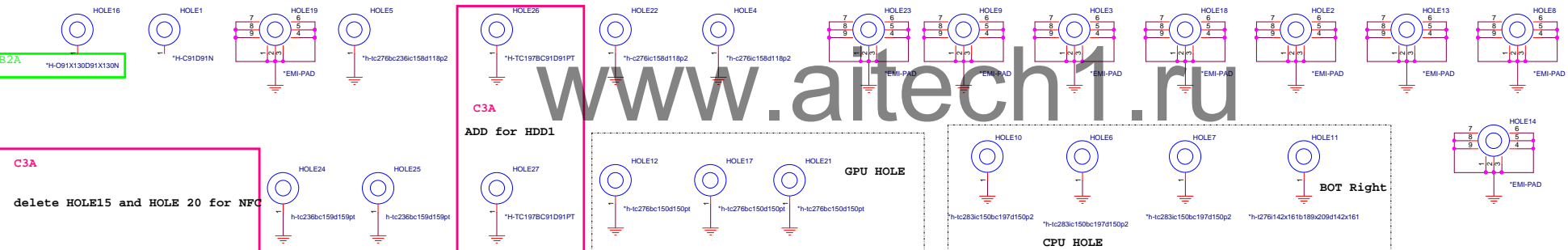
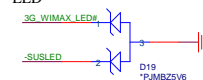


ESD Protect LED

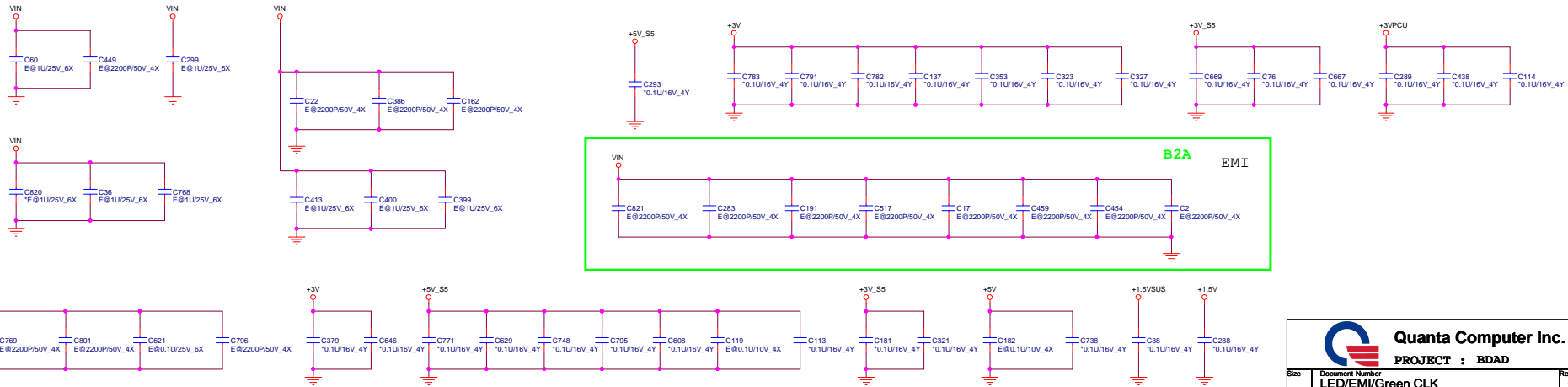
FOR BATTERY LED



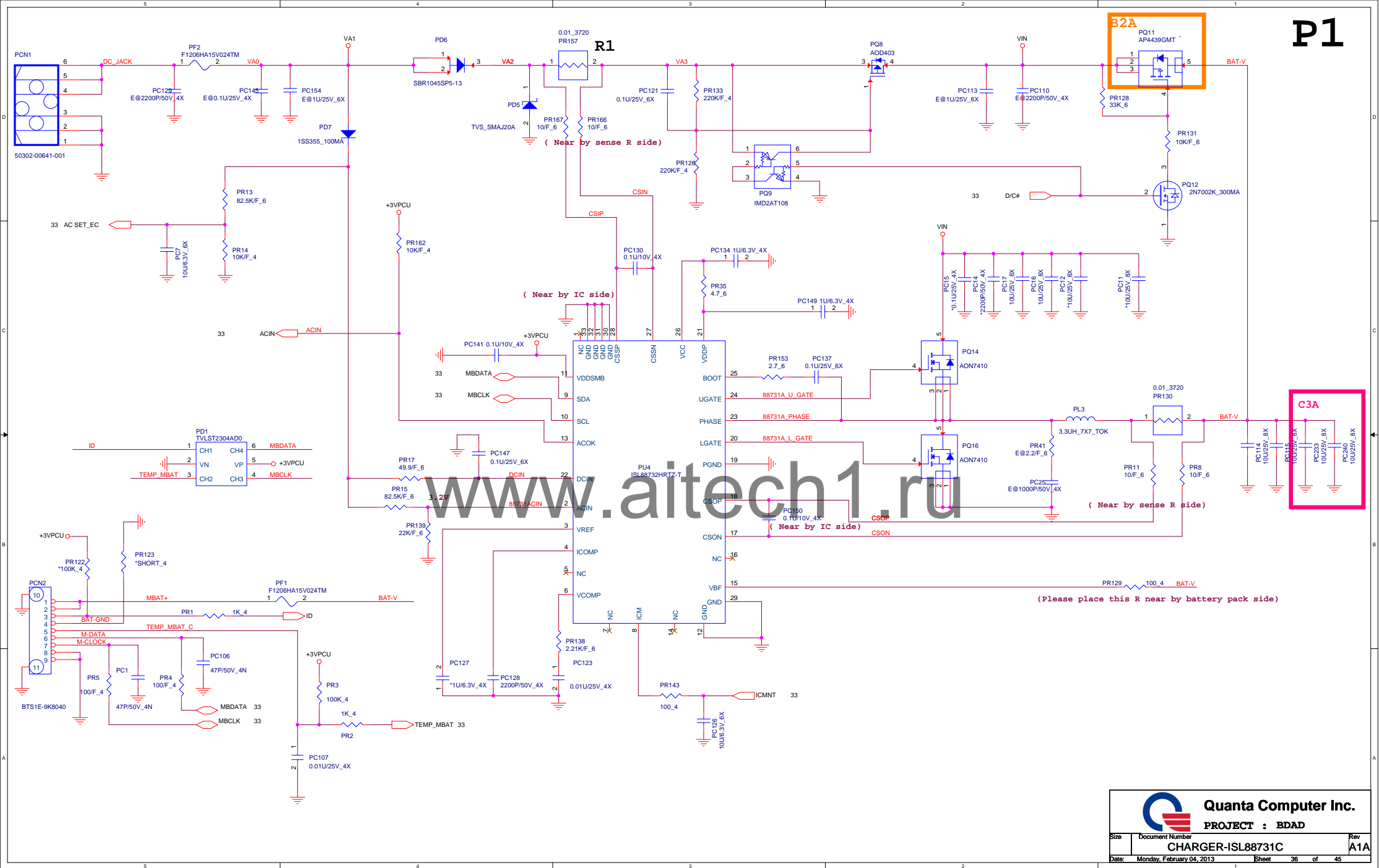
FOR W-LAN&POWER LED



EMI EMI



P1



Quanta Computer Inc.
PROJECT : BDAD

Size: Document Number: CHARGER-ISL88731C Rev: A1A
Date: Monday, February 04, 2013 Sheet: 36 of 45

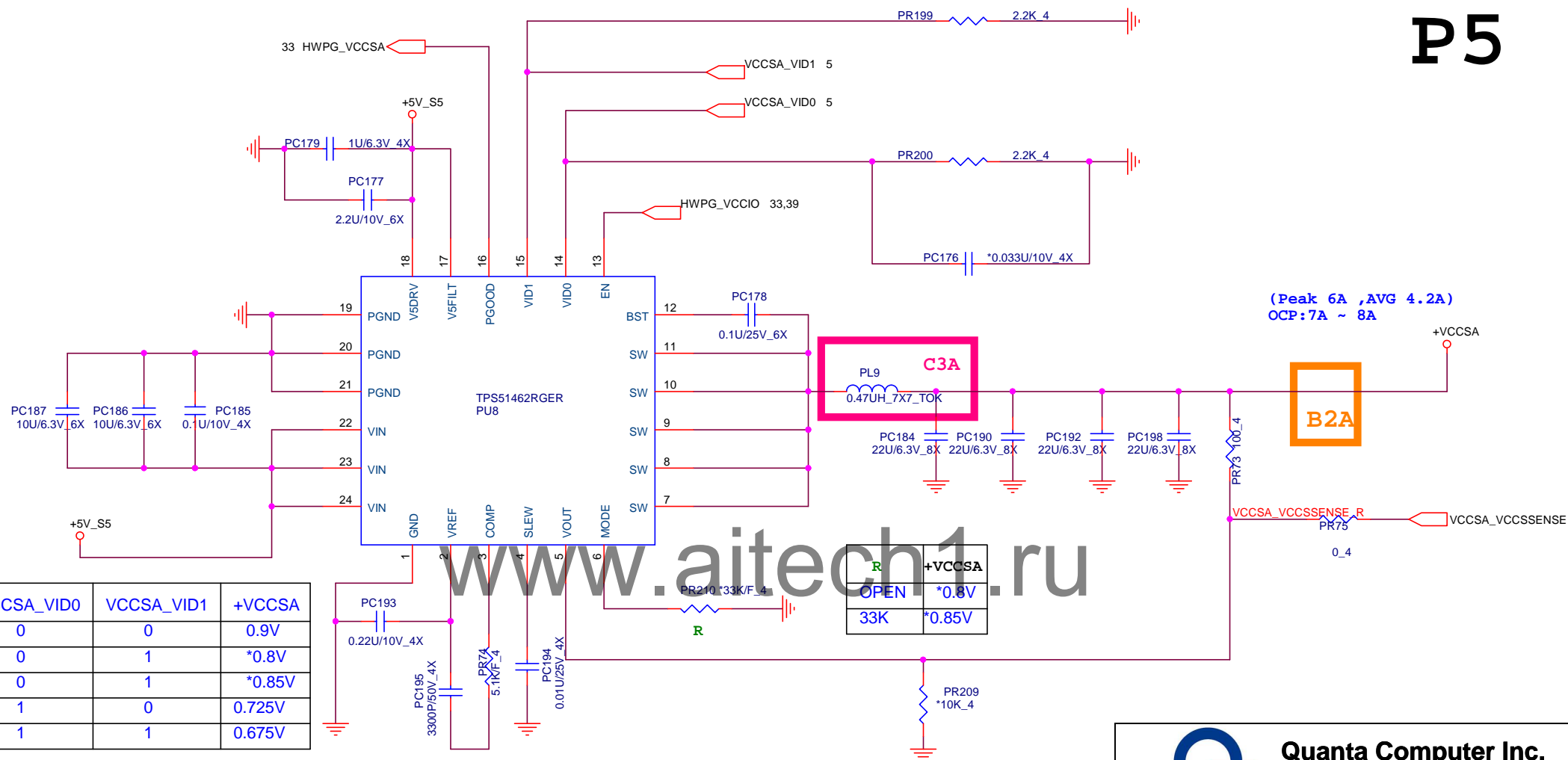





$$V_{OUT} = (1 + R_1/R_2) * 0.5$$
**Quanta Computer Inc.**

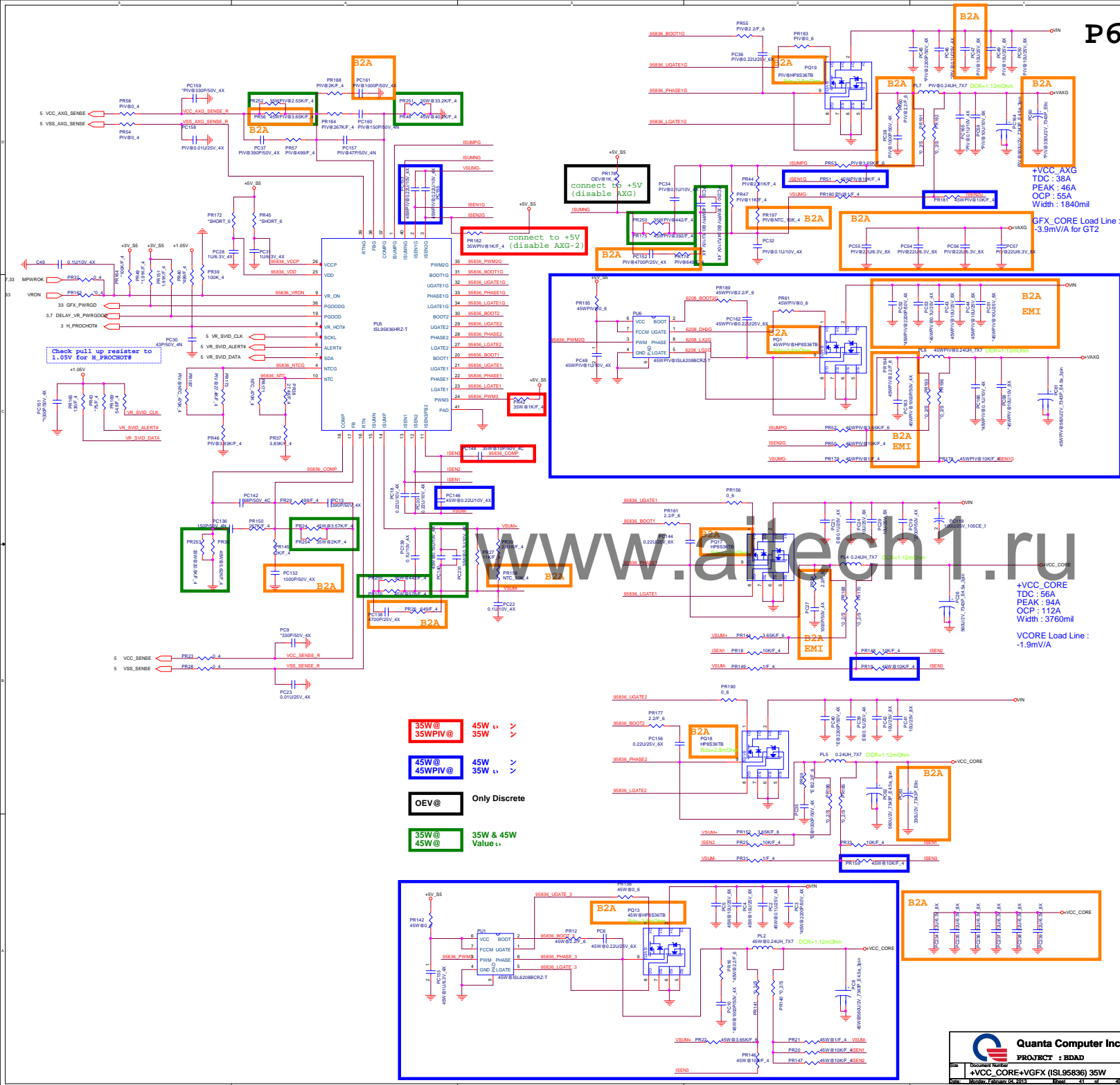
PROJECT : BDAD

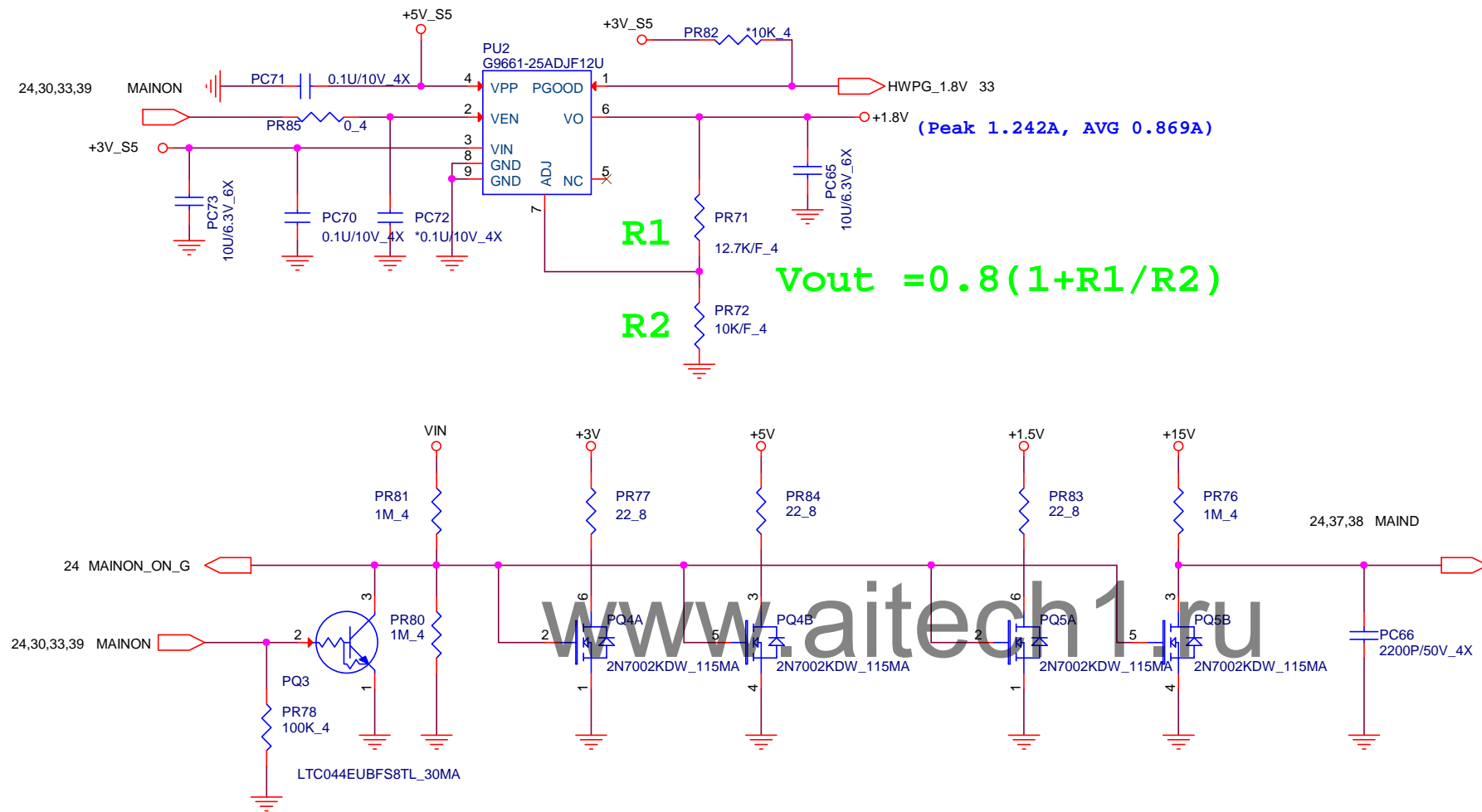
Size	Document Number +VCCIO(RT8240BGQW)	Rev A1A
Date:	Mondav. Februarv 04. 2013	Sheet 39 of 45




VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

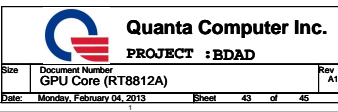
*0.8V FOR SV TYPE
*0.85V FOR LV/ULV TYPE

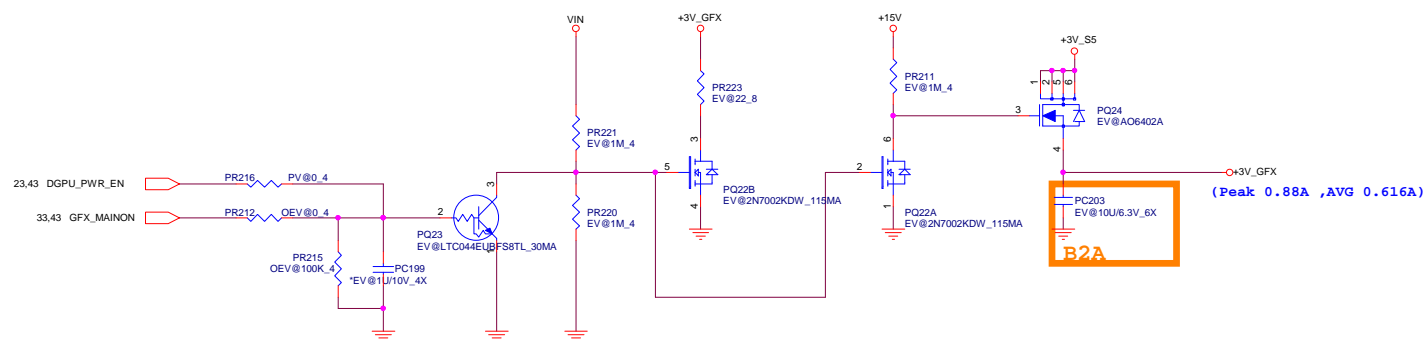
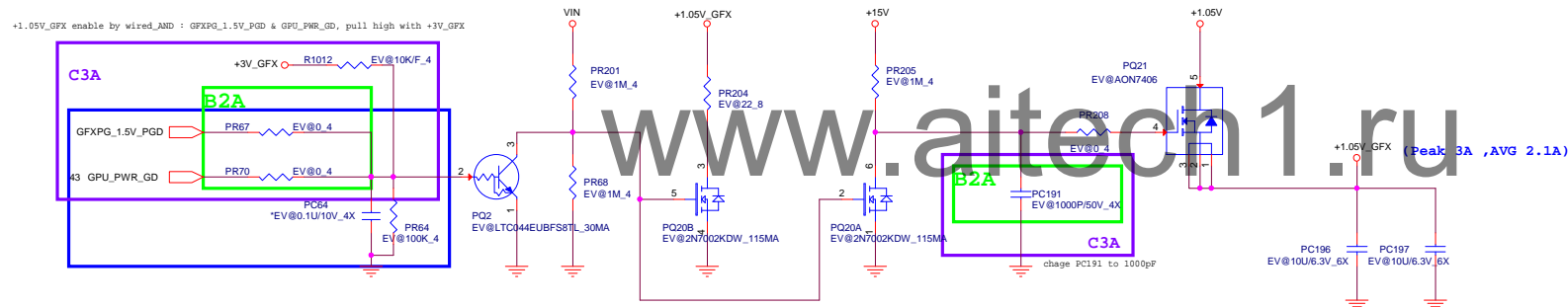
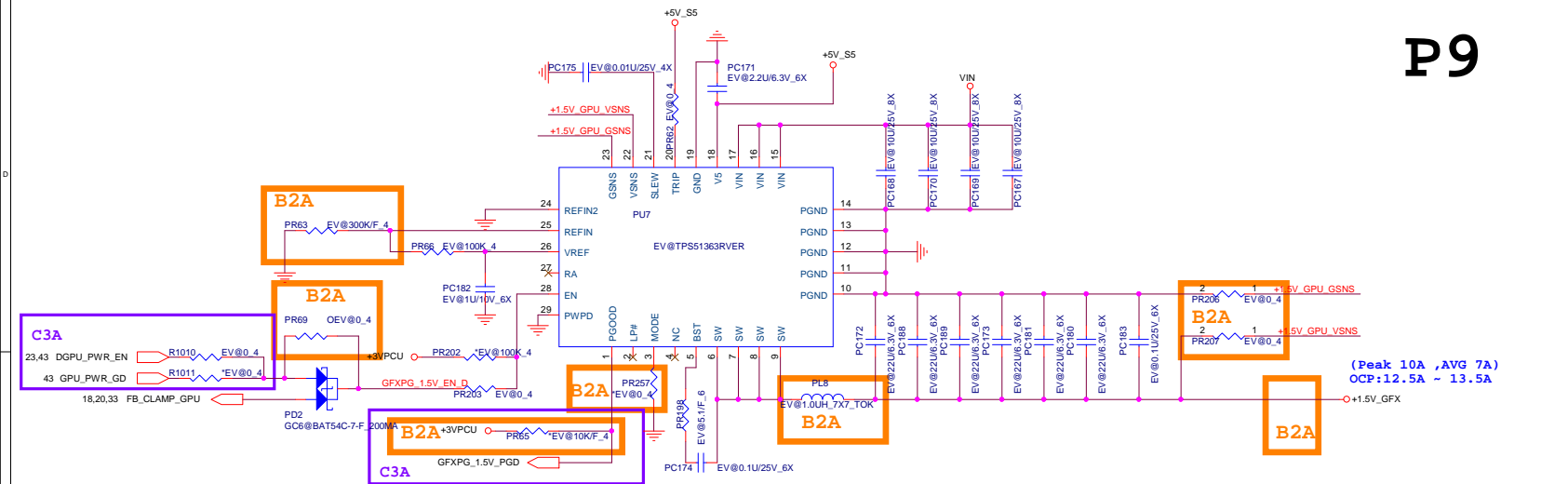




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 Quanta Computer Inc. PROJECT : BDAD	
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+1.8V/Discharge	
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GPU Power On Sequence

1. DGPU_PWR_EN_R(delay) Enable +3V_GFX from +3V_S5
2. DGPU_PWR_EN Enable +VGPU_CORE
3. GPU_PWR_GD Enable +1.5V_GFX
4. GPU_PWR_GD Enable(Delay) +1.05V_GFX

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